

Title	Page
Cover Sheet	1
Block Diagram	2
Device Map	3
GPIO Table	4
Clock Distribution	5
CPU:LGA 1156	6 - 12
DDR III DIMM	13 - 17
CLK-Gen Silego SLG8SP585	18
INTEL-IBEXPEAK PCH	19 - 26
IO-Fintek F71858D	27
PCIE X16 SLOT	28
PCIE X1 SLOT	29
Mini PCI_E Slot & ONFI Slot	30
1394 Controller - VT6315N	31
LAN-RTL8111DL	32
Audio Codec ALC888S	33, 34 ,35
VGA	36
DVI transfer	37
FAN Control	38
USB Conn.	39, 40
ACPI Controller	41, 42
DDR, CPU (VCCP/VGUP/VTT) & PCH Power	43 - 47
ATX PWR-Connector/LED	48
CPU/PCH XDP	49
Manual & Option parts	50
Power Map/History	51, 52, 53

MS-7613 Ver: 10 uATX(244mm X 244mm)

CPU:

INTEL -Clarkdale/Lynnfied LGA 1156

System Chipset:

INTEL-IBEXPEAK PCH

OnBoard Chipset:

Clock Gen:Silego SLG8SP585

HD Audio Codec:ALC888S

LAN:RTL8111DL 10/100/1000

IO: Fintek F71858D

Flash ROM: 32 Mb SPI (CHIP) Fire wire: VIA VT6315N

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 3

Mini PCI Express (X1) Slot * 1

ONFI Slot *1

PWM:

Controller:Intersil ISL6333 3-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *6

USB2.0 *14 (Rear*6 / Front*8)

on BOARD BUZZER

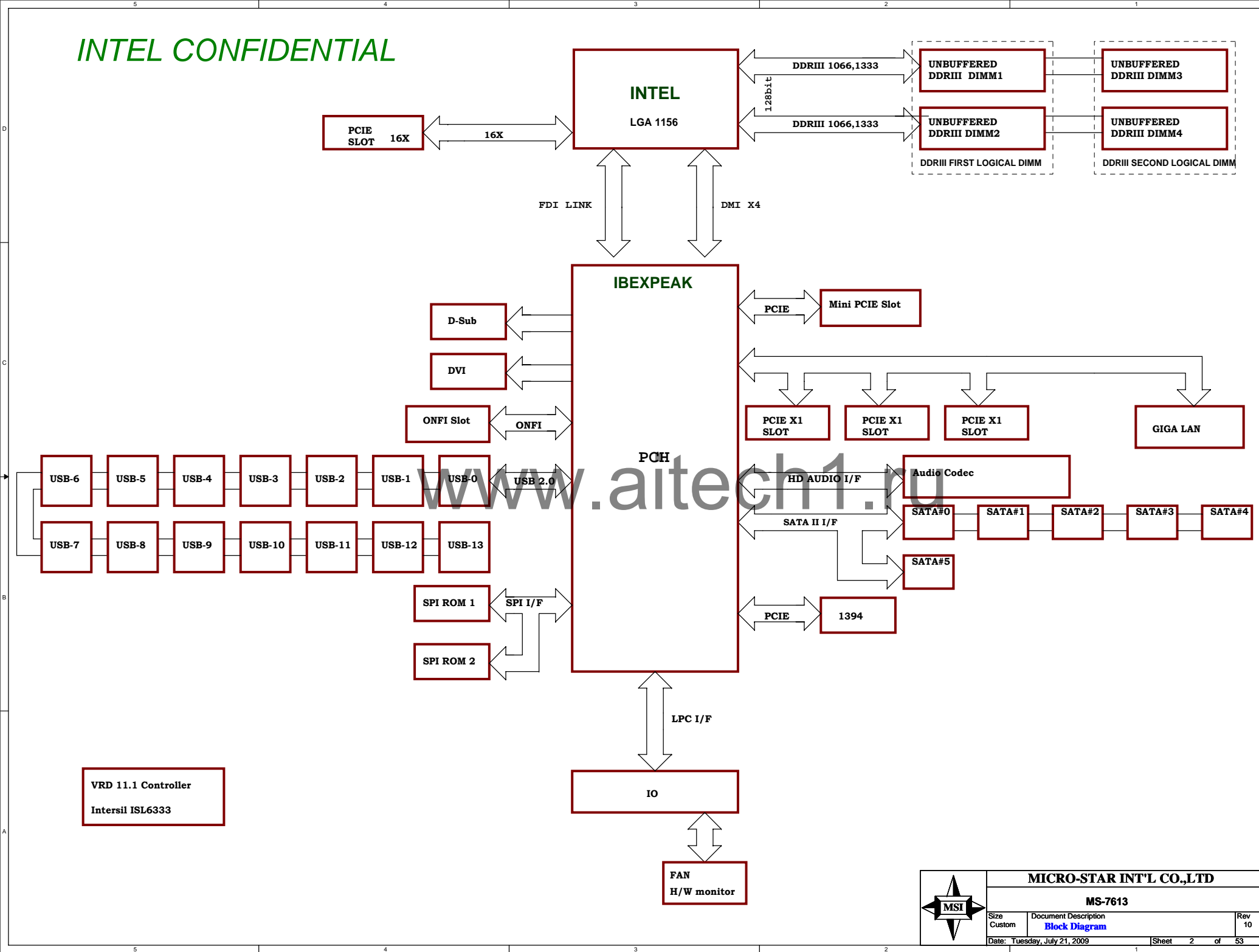
D-SUB *1

DVI PORT*1



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size Custom	Document Description Cover Sheet	Rev 10
Date: Tuesday, July 21, 2009		Sheet 1 of 53

INTEL CONFIDENTIAL



MICRO-STAR INT'L CO.,LTD

MS-7613

Size Custom	Document Description Block Diagram	Rev 10
Date: Tuesday, July 21, 2009	Sheet 2 of 53	

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1

TABLE 9↓
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #3	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes



				18BXPSAK GPIO DEFINITION	
GPIO	POWER	IO	Function	Implementation	Mother board Function
GPIO0	MAIN	1	BMBUSY#	10 K Pull-up to +3.3V	ADPT_ID_DET#
GPIO1	MAIN	1	TACH1	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH1
GPIO2	MAIN	1	PCLIRQB#	See PCA Spec	PCI Interrupt E#
GPIO3	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt F#
GPIO4	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt G#
GPIO5	MAIN	1	PCLIRQ#	See PCA Spec	PCI Interrupt H#
GPIO6	MAIN	1	TACH2	Pull-up to +3.3V and connect to P52 pin 12. The COM18 Assembly connects pin 12 directly to GND	COMM_8_DET#/ MOM_TH_ALRT#
GPIO7	MAIN	1	TACH3	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH3(PSU Fan Control)
GPIO8	RESUMB	0	ICG_B#		Reserved
GPIO9	RESUMB	1	OC5	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO10	RESUMB	1	OC6	10K Pull-up to +3.3V and connect to P126-pin 16	PRNTR_DET#
GPIO11	RESUMB	1	SMBALERT#	20K Pull-up to +3.3VSB. It is always enabled as a wake event.	SMBALERT#
GPIO12	RESUMB	1	LAN_DISABLE	Follow implementation in Intel Picton Design Guide	LAN_DISABLE#
GPIO13	RESUMB	1	IO_PMB	10K Pull-up to +3.3V and connect to P151-pin 10; also add a no-installed pull-down to the net.	RDYBST_DET# or DASH SMI
GPIO14	RESUMB	1	OC7	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation. 8.2K Pull-up to +3.3V and connect to the SMI pin on the SIO	SMI# from SIO
GPIO15	RESUMB	1	PCB_GPIO5		Reserved
GPIO16	RESUMB	0	SATA2DP	10 M pull-up to VBAT and connect to CPU SKT0CC#, SIO pin48 and PCH	CPU_MISSING
GPIO17	MAIN	1	TACH0	connect through a 0Ω series resistor, and refer the PCA spec for Fans mapping, if not used by the system then 10K pull-up to +3.3V.	TACH0(Front Chassis Fan)
GPIO18	MAIN	1	PCIECLKQ#	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to E15-pin 1. E15 Pin 2 connect to GND	BOOT_BLK_REC#
GPIO19	MAIN	1	SATA1QP	connect to a test point	unused
GPIO20	MAIN	1	PCIECLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to HANKSVILLE -pin48	PCIECLKQ2#
GPIO21	MAIN	1	SATA2QP	10K pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#
GPIO22	MAIN	1	SCLOCK	10K Pull-up to +3.3V and connect to P160-pin 10	INT_USB_DET#
GPIO23	MAIN	1	LDQ#	connect to a test point.	PEG_MOM_DET#
GPIO24	RESUMB	0	MBALED	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to P125-Pin 1. 1M pull-up to VBAT and connect to P125-pin 3	HOOD_SW_DET#
GPIO25	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ3#
GPIO26	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ4#
GPIO27	RESUMB	0	OD_PLL_VR_EN	10K pull-up to +3.3VAUX	Reserved
GPIO28	RESUMB	0	PCB_GP28	connect to a test point	unused
GPIO29	RESUMB	0	SLP_LAN#	refer to the PCA spec.	SLP_LAN#
GPIO30	RESUMB	1	SUS_PWR_ACK	100K Pull-up to 3V_AUX	unused
GPIO31	MAIN	1	ACPRESENT	10K Pull-up to +3.3V and connect to P25-pin 10	FRONT_USB_DET1#
GPIO32	MAIN	0	PCB_GP12	Through a 1kΩ series resistor, 10K pull-up to +3.3V and connect to P2-pin 6.	NON-EPA_PS_DET#

GPIO33	MAIN	0	PCB_GP33	Through a 1kΩ series resistor, 8.2K pull-up to +3.3V and connect to pin 1 of jumper E1 and E1 pin2 to GND	FDT_OVRD#
GPIO34	MAIN	0	SP_PC#	3.3K Pull-down to GND and connect to P124-pin 2. Decouple P124-pin 2 with 0.1μF P124 pin 1 2.2K pull-up to 5V and P124 pin 6 2.2K pull-up to 5V	HOOD_LOCK_DET
GPIO35	MAIN	0	SATACLKREQ#	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0
GPIO36	MAIN	1	SATA2QP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1
GPIO37	MAIN	1	SATA3QP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2
GPIO38	MAIN	1	SLOAD	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 9. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID0
GPIO39	MAIN	1	SDATAOUT0	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BRD_ID1
GPIO40	RESUMB	1	OC1	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for XDP implementation. 8.2kΩ pull-down to GND and connect to E49-pin 2 E49 pin-1 300 pull-up to +3.3V	PASSWORD_EN
GPIO41	RESUMB	1	OC2	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO42	RESUMB	1	OC3	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO43	RESUMB	1	OC4	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO44	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3VAUX and connect to a test point.	PCIECLKQ6#
GPIO45	RESUMB	1	PCIECLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J3-pin8 I7	PRSN#_J31
GPIO46	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3V and connect to a test point.	PCIECLKQ7#
GPIO47	RESUMB	1	PBG_A_CLKQ#	Through a 0Ω series resistor, 10K pull-up to +3.3V and connect to J4-pin848 and B81	PRSN#_J41
GPIO48	MAIN	1	SDATAOUT1	Through a series 1K resistor, 10K Pull-up to +3.3V and 10K pull-down to GND and connect to P5-pin 10. See PCA spec to determine the stuffing requirements for these resistors.	CHASSIS_ID1
GPIO49	MAIN	0	SATA3QP	10K Pull-up to +3.3V and 10K pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0
GPIO50	MAIN	1	PCLIRQ#1	8.2k pull-up to VCC3	REQ1#
GPIO51	MAIN	0	PCLQNT#1	connect to a test point	GNT1#
GPIO52	MAIN	1	PCLIRQ#2	8.2k pull-up to VCC3	REQ2#
GPIO53	MAIN	0	PCLQNT#2	connect to a test point	GNT2#
GPIO54	MAIN	1	PCLIRQ#3	Through a 8.2KΩ series resistor, connect to E14-pin 2 and 1K pull-down to GND. E14-pin1 connect to +3.3V	BOOT_BLK_EN#
GPIO55	MAIN	0	PCLQNT#3	connect to a test point	GNT3#
GPIO56	RESUMB	1	PBG_B_CLKQ#	refer to the PCA spec.	AUD_AMP_DIS#
GPIO57	MAIN	1	PCB_GP57	10K Pull-up to +3.3VME installed and 10K pull-down to GND not installed.	TPM_PP

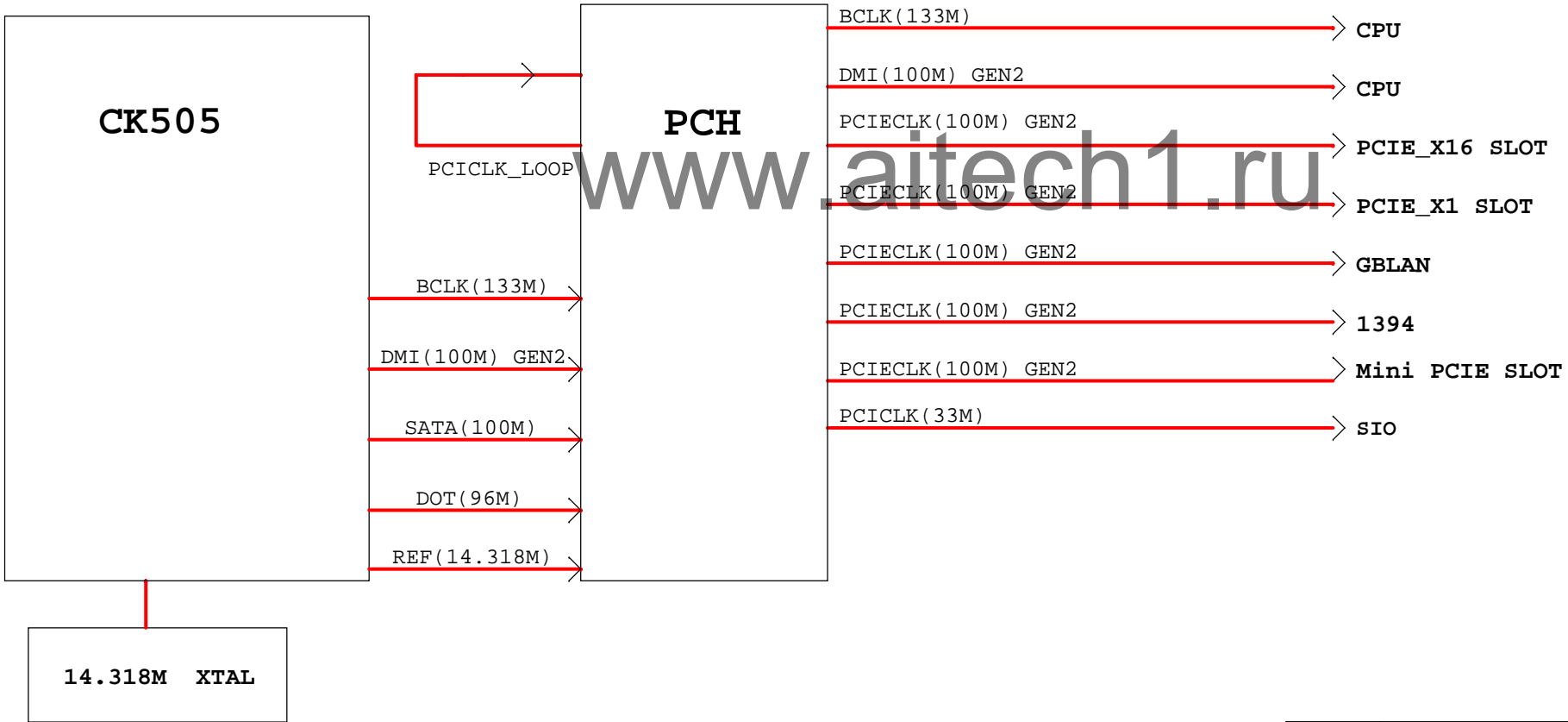
GPIO58	RESUMB	0	SMCLK	10K pull-up to 3V_AUX	SMCLK
GPIO59	RESUMB	1	OC0	connect through a 0Ω series resistor to XDP and system GPIO function. Refer the XDP design guide for xdp implementation.	USB_OC#
GPIO60	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALARM
GPIO61	RESUMB	0	SUS_STAT#	connect to a test pin	LPCPD#
GPIO62	RESUMB	0	SUSCLK	SUSCLK to SIO-pin16	SUSCLK
GPIO63	RESUMB	0	SLP_S#	Connect to the SIO-pin37	SLP_S#
GPIO64	MAIN	0	CLKOUTFLBK0	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK0
GPIO65	MAIN	0	CLKOUTFLBK1	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK1
GPIO66	MAIN	0	CLKOUTFLBK2	refer to the PCA spec. unused clock connect to a test point	CLKOUTFLBK2
GPIO67	MAIN	0	CLKOUTFLBK3	refer to the PCA spec. unused clock connect to a test point	CLK14M
GPIO72	RESUMB	1	PCB_GP72	Pull-up to +3.3V and connect to P24-pin 10	FRONT_USB_DET0#
GPIO73	RESUMB	1	PCIECLKQ#	10K pull-up to +3.3VAUX and through a 0Ω series resistor, connect to J42-pin8 I7, B31, B48, and B81	PRSN#_J42
GPIO74	RESUMB	0	SMDALBRT#	10K pull-up to 3V_AUX	SMDALERT#
GPIO75	RESUMB	0	SMDLIDATA	10K pull-up to 3V_AUX	SMDLIDATA



MICRO-STAR INT'L CO.,LTD

MS-7613

Size Custom	Document Description PCH GPIO Table	Rev 10
Date: Tuesday, July 21, 2009		Sheet 4 of 53



Size Custom	Document Description CPU-CLK/Control/MISC	Rev 10
Date: Tuesday, July 21, 2009		Sheet 6 of 53

13,14 MEM_MA_DATA[63..0]

13,14 MEM_MA_ADD[15..0]

13,14 MEM_MA_WE_L
13,14 MEM_MA_CAS_L
13,14 MEM_MA_RAS_L

13,14 MEM_MA_BANK0
13,14 MEM_MA_BANK1
13,14 MEM_MA_BANK2

13 MEM_MA_CS_L0
13 MEM_MA_CS_L1
14 MEM_MA_CS_L2
14 MEM_MA_CS_L3

13 MEM_MA_CKE0
13 MEM_MA_CKE1
14 MEM_MA_CKE2
14 MEM_MA_CKE3

13 MEM_MA_ODT0
13 MEM_MA_ODT1
14 MEM_MA_ODT2
14 MEM_MA_ODT3

13 MEM_MA_CLK_H0
13 MEM_MA_CLK_L0
13 MEM_MA_CLK_H1
14 MEM_MA_CLK_L1
14 MEM_MA_CLK_H2
14 MEM_MA_CLK_L2
14 MEM_MA_CLK_H3
14 MEM_MA_CLK_L3

13,14,15,16 DDR3_DRAMRST#

CPU1A

MEM_MA_ADD0 AW18
MEM_MA_ADD1 AY15
MEM_MA_ADD2 AV15
MEM_MA_ADD3 AU15
MEM_MA_ADD4 AW14
MEM_MA_ADD5 AV13
MEM_MA_ADD6 AV14
MEM_MA_ADD7 AW13
MEM_MA_ADD8 AU14
MEM_MA_ADD9 AW12
MEM_MA_ADD10 AT18
MEM_MA_ADD11 AU13
MEM_MA_ADD12 AW11
MEM_MA_ADD13 AU24
MEM_MA_ADD14 AT11
MEM_MA_ADD15 AU10

MEM_MA_WE_L AT22
MEM_MA_CAS_L AU22
MEM_MA_RAS_L AT20

MEM_MA_BANK0 AV20
MEM_MA_BANK1 AU19
MEM_MA_BANK2 AU12

MEM_MA_CS_L0 AV21
MEM_MA_CS_L1 AW24
MEM_MA_CS_L2 AU21
MEM_MA_CS_L3 AU23

MEM_MA_CKE0 AU10
MEM_MA_CKE1 AU10
MEM_MA_CKE2 AV10
MEM_MA_CKE3 AY10

MEM_MA_ODT0 AV23
MEM_MA_ODT1 AV24
MEM_MA_ODT2 AW23
MEM_MA_ODT3 AY24

MEM_MA_CLK_H0 AR22
MEM_MA_CLK_L0 AR21
MEM_MA_CLK_H1 AP18
MEM_MA_CLK_L1 AN18
MEM_MA_CLK_H2 AN21
MEM_MA_CLK_L2 AP21
MEM_MA_CLK_H3 AP19
MEM_MA_CLK_L3 AN19

DDR3_DRAMRST# AV8
SM_DRAMRST#

AK22 SA_CS[4]*
AM22 SA_CS[5]*
AL23 SA_CS[6]*
AK23 SA_CS[7]*

AL10 SA_DQS[8]
AM10 SA_DQS[8]*

AP10 SA_ECC_CB[0]
AN10 SA_ECC_CB[1]
AR11 SA_ECC_CB[2]
AP11 SA_ECC_CB[3]
AK9 SA_ECC_CB[4]
AL9 SA_ECC_CB[5]
AK11 SA_ECC_CB[6]
AM11 SA_ECC_CB[7]

DDR_A

1 OF 12

SA_DQS[0] AK3
SA_DQS[0]* AJ3
SA_DM[0] AJ2
SA_DQ[0] AH1
SA_DQ[1] AJ4
SA_DQ[1] AL2
SA_DQ[2] AL1
SA_DQ[3] AG2
SA_DQ[4] AH2
SA_DQ[5] AK1
SA_DQ[6] AK2
SA_DQ[7] AP2
SA_DQS[1] AP3
SA_DQS[1]* AN1
SA_DM[1] AN3
SA_DQ[8] AN2
SA_DQ[9] AR3
SA_DQ[10] AR2
SA_DQ[11] AM3
SA_DQ[12] AM2
SA_DQ[13] AP1
SA_DQ[14] AR4
SA_DQ[15] AU4
SA_DQS[2] AU3
SA_DQS[2]* AU1
SA_DM[2] AT4
SA_DQ[16] AU2
SA_DQ[17] AU3
SA_DQ[18] AU4
SA_DQ[19] AT3
SA_DQ[20] AT1
SA_DQ[21] AV2
SA_DQ[22] AV4
SA_DQ[23] AY6
SA_DQS[3] AW6
SA_DQS[3]* AV6
SA_DM[3] AW5
SA_DQ[24] AY5
SA_DQ[25] AU8
SA_DQ[26] AU8
SA_DQ[27] AU8
SA_DQ[28] AU5
SA_DQ[29] AV7
SA_DQ[30] AW7
SA_DQ[31] AR28
SA_DQS[4] AR29
SA_DQS[4]* AN29
SA_DM[4] AN27
SA_DQ[32] AT28
SA_DQ[33] AP28
SA_DQ[34] AP30
SA_DQ[35] AN26
SA_DQ[36] AR27
SA_DQ[37] AR29
SA_DQ[38] AN30
SA_DQ[39] AV32
SA_DQS[5] AW32
SA_DQS[5]* AW31
SA_DM[5] AU30
SA_DQ[40] AU31
SA_DQ[41] AV33
SA_DQ[42] AU34
SA_DQ[43] AV30
SA_DQ[44] AV30
SA_DQ[45] AU33
SA_DQ[46] AW33
SA_DQ[47] AW36
SA_DQS[6] AV35
SA_DQS[6]* AU35
SA_DM[6] AW35
SA_DQ[48] AY35
SA_DQ[49] AV37
SA_DQ[50] AU37
SA_DQ[51] AY34
SA_DQ[52] AW34
SA_DQ[53] AV36
SA_DQ[54] AW37
SA_DQ[55] AR39
SA_DQS[7] AR38
SA_DQS[7]* AT38
SA_DM[7] AT39
SA_DQ[56] AT40
SA_DQ[57] AN38
SA_DQ[58] AN39
SA_DQ[59] AU38
SA_DQ[60] AU39
SA_DQ[61] AP39
SA_DQ[62] AP40
SA_DQ[63] AT39

MEM_MA_DQS_H0
MEM_MA_DQS_L0
MEM_MA_DM0
MEM_MA_DATA0
MEM_MA_DATA1
MEM_MA_DATA2
MEM_MA_DATA3
MEM_MA_DATA4
MEM_MA_DATA5
MEM_MA_DATA6
MEM_MA_DATA7
MEM_MA_DQS_H1
MEM_MA_DQS_L1
MEM_MA_DM1
MEM_MA_DATA8
MEM_MA_DATA9
MEM_MA_DATA10
MEM_MA_DATA11
MEM_MA_DATA12
MEM_MA_DATA13
MEM_MA_DATA14
MEM_MA_DATA15
MEM_MA_DQS_H2
MEM_MA_DQS_L2
MEM_MA_DM2
MEM_MA_DATA16
MEM_MA_DATA17
MEM_MA_DATA18
MEM_MA_DATA19
MEM_MA_DATA20
MEM_MA_DATA21
MEM_MA_DATA22
MEM_MA_DATA23
MEM_MA_DQS_H3
MEM_MA_DQS_L3
MEM_MA_DM3
MEM_MA_DATA24
MEM_MA_DATA25
MEM_MA_DATA26
MEM_MA_DATA27
MEM_MA_DATA28
MEM_MA_DATA29
MEM_MA_DATA30
MEM_MA_DATA31
MEM_MA_DQS_H4
MEM_MA_DQS_L4
MEM_MA_DM4
MEM_MA_DATA32
MEM_MA_DATA33
MEM_MA_DATA34
MEM_MA_DATA35
MEM_MA_DATA36
MEM_MA_DATA37
MEM_MA_DATA38
MEM_MA_DATA39
MEM_MA_DQS_H5
MEM_MA_DQS_L5
MEM_MA_DM5
MEM_MA_DATA40
MEM_MA_DATA41
MEM_MA_DATA42
MEM_MA_DATA43
MEM_MA_DATA44
MEM_MA_DATA45
MEM_MA_DATA46
MEM_MA_DATA47
MEM_MA_DQS_H6
MEM_MA_DQS_L6
MEM_MA_DM6
MEM_MA_DATA48
MEM_MA_DATA49
MEM_MA_DATA50
MEM_MA_DATA51
MEM_MA_DATA52
MEM_MA_DATA53
MEM_MA_DATA54
MEM_MA_DATA55
MEM_MA_DQS_H7
MEM_MA_DQS_L7
MEM_MA_DM7
MEM_MA_DATA56
MEM_MA_DATA57
MEM_MA_DATA58
MEM_MA_DATA59
MEM_MA_DATA60
MEM_MA_DATA61
MEM_MA_DATA62
MEM_MA_DATA63

N12-156A010-F02



MICRO-STAR INT'L CO.,LTD

MS-7613

Size	Document Description	Rev
Custom	CPU-Memory CH-A	10
Date: Tuesday, July 21, 2009		
Sheet 7 of 53		

15,16 MEM_MB_DATA[63..0]

15,16 MEM_MB_ADD[15..0]

CPU1B

15,16 MEM_MB_WE_L

15,16 MEM_MB_CAS_L

15,16 MEM_MB_RAS_L

15,16 MEM_MB_BANK0

15,16 MEM_MB_BANK1

15,16 MEM_MB_BANK2

15 MEM_MB_CS_L0

15 MEM_MB_CS_L1

16 MEM_MB_CS_L2

16 MEM_MB_CS_L3

15 MEM_MB_CKE0

15 MEM_MB_CKE1

16 MEM_MB_CKE2

16 MEM_MB_CKE3

15 MEM_MB_ODT0

15 MEM_MB_ODT1

16 MEM_MB_ODT2

16 MEM_MB_ODT3

15 MEM_MB_CLK_H0

15 MEM_MB_CLK_L0

15 MEM_MB_CLK_H1

15 MEM_MB_CLK_L1

16 MEM_MB_CLK_H2

16 MEM_MB_CLK_L2

16 MEM_MB_CLK_H3

16 MEM_MB_CLK_L3

MEM_MB_ADD0 AU20
MEM_MB_ADD1 AU18
MEM_MB_ADD2 AV18
MEM_MB_ADD3 AU17
MEM_MB_ADD4 AY18
MEM_MB_ADD5 AV17
MEM_MB_ADD6 AW17
MEM_MB_ADD7 AU16
MEM_MB_ADD8 AT17
MEM_MB_ADD9 AY16
MEM_MB_ADD10 AY25
MEM_MB_ADD11 AW16
MEM_MB_ADD12 AW15
MEM_MB_ADD13 AW28
MEM_MB_ADD14 AY12
MEM_MB_ADD15 AV11
SB_MA[0]
SB_MA[1]
SB_MA[2]
SB_MA[3]
SB_MA[4]
SB_MA[5]
SB_MA[6]
SB_MA[7]
SB_MA[8]
SB_MA[9]
SB_MA[10]
SB_MA[11]
SB_MA[12]
SB_MA[13]
SB_MA[14]
SB_MA[15]

MEM_MB_WE_L AU26
MEM_MB_CAS_L AW27
MEM_MB_RAS_L AW26
SB_WE*
SB_CAS*
SB_RAS*

MEM_MB_BANK0 AU25
MEM_MB_BANK1 AW25
MEM_MB_BANK2 AV12
SB_BA[0]
SB_BA[1]
SB_BA[2]

MEM_MB_CS_L0 AY27
MEM_MB_CS_L1 AW29
MEM_MB_CS_L2 AV26
MEM_MB_CS_L3 AV29
SB_CS[0]*
SB_CS[1]*
SB_CS[2]*
SB_CS[3]*

MEM_MB_CKE0 AW8
MEM_MB_CKE1 AY9
MEM_MB_CKE2 AU9
MEM_MB_CKE3 AV9
SB_CKE[0]
SB_CKE[1]
SB_CKE[2]
SB_CKE[3]

MEM_MB_ODT0 AU27
MEM_MB_ODT1 AU29
MEM_MB_ODT2 AW27
MEM_MB_ODT3 AU28
SB_ODT[0]
SB_ODT[1]
SB_ODT[2]
SB_ODT[3]

MEM_MB_CLK_H0 AR17
MEM_MB_CLK_L0 AR16
MEM_MB_CLK_H1 AT15
MEM_MB_CLK_L1 AR15
MEM_MB_CLK_H2 AN17
MEM_MB_CLK_L2 AN16
MEM_MB_CLK_H3 AR19
MEM_MB_CLK_L3 AR18
SB_CK[0]
SB_CK[1]
SB_CK[2]
SB_CK[3]
SB_CK[4]
SB_CK[5]
SB_CK[6]
SB_CK[7]

AM23
AM24
AL24
AK24
SB_CS[4]*
SB_CS[5]*
SB_CS[6]*
SB_CS[7]*

AR14
AR13
SB_DQS[8]
SB_DQS[8]*

AR12
AT13
AN15
AP14
AM12
AN12
AN14
AP13
SB_ECC_CB[0]
SB_ECC_CB[1]
SB_ECC_CB[2]
SB_ECC_CB[3]
SB_ECC_CB[4]
SB_ECC_CB[5]
SB_ECC_CB[6]
SB_ECC_CB[7]

DDR_B

2 OF 12

SB_DQS[0] AF4 MEM_MB_DQS_H0
SB_DQS[0]* AE5 MEM_MB_DQS_L0
SB_DM[0] AE4 MEM_MB_DM0
MEM_MB_DQS_H0 15,16
MEM_MB_DQS_L0 15,16
MEM_MB_DM0 15,16
AD7 MEM_MB_DATA0
AD6 MEM_MB_DATA1
AH8 MEM_MB_DATA2
AJ8 MEM_MB_DATA3
AC7 MEM_MB_DATA4
AC6 MEM_MB_DATA5
AE5 MEM_MB_DATA6
AE6 MEM_MB_DATA7
SB_DQ[0]
SB_DQ[1]
SB_DQ[2]
SB_DQ[3]
SB_DQ[4]
SB_DQ[5]
SB_DQ[6]
SB_DQ[7]
AH6 MEM_MB_DQS_H1
AJ5 MEM_MB_DQS_L1
AH4 MEM_MB_DM1
MEM_MB_DQS_H1 15,16
MEM_MB_DQS_L1 15,16
MEM_MB_DM1 15,16
AG5 MEM_MB_DATA8
AH7 MEM_MB_DATA9
AK6 MEM_MB_DATA10
AL4 MEM_MB_DATA11
AG6 MEM_MB_DATA12
AG4 MEM_MB_DATA13
AJ7 MEM_MB_DATA14
AK7 MEM_MB_DATA15
SB_DQ[8]
SB_DQ[9]
SB_DQ[10]
SB_DQ[11]
SB_DQ[12]
SB_DQ[13]
SB_DQ[14]
SB_DQ[15]
AN6 MEM_MB_DQS_H2
AM6 MEM_MB_DQS_L2
AM7 MEM_MB_DM2
MEM_MB_DQS_H2 15,16
MEM_MB_DQS_L2 15,16
MEM_MB_DM2 15,16
AL6 MEM_MB_DATA16
AN5 MEM_MB_DATA17
AP6 MEM_MB_DATA18
AR5 MEM_MB_DATA19
AL5 MEM_MB_DATA20
AM4 MEM_MB_DATA21
AN7 MEM_MB_DATA22
AP5 MEM_MB_DATA23
SB_DQ[16]
SB_DQ[17]
SB_DQ[18]
SB_DQ[19]
SB_DQ[20]
SB_DQ[21]
SB_DQ[22]
SB_DQ[23]
AR8 MEM_MB_DQS_H3
AP8 MEM_MB_DQS_L3
AT7 MEM_MB_DM3
MEM_MB_DQS_H3 15,16
MEM_MB_DQS_L3 15,16
MEM_MB_DM3 15,16
AT6 MEM_MB_DATA24
AR7 MEM_MB_DATA25
SB_DQ[24]
SB_DQ[25]
SB_DQ[26]
SB_DQ[27]
SB_DQ[28]
SB_DQ[29]
SB_DQ[30]
SB_DQ[31]
AT25 MEM_MB_DQS_H4
AR24 MEM_MB_DQS_L4
AN24 MEM_MB_DM4
MEM_MB_DQS_H4 15,16
MEM_MB_DQS_L4 15,16
MEM_MB_DM4 15,16
AN23 MEM_MB_DATA32
AP23 MEM_MB_DATA33
AR25 MEM_MB_DATA34
AR26 MEM_MB_DATA35
AT23 MEM_MB_DATA36
AP22 MEM_MB_DATA37
AP25 MEM_MB_DATA38
AT26 MEM_MB_DATA39
SB_DQ[32]
SB_DQ[33]
SB_DQ[34]
SB_DQ[35]
SB_DQ[36]
SB_DQ[37]
SB_DQ[38]
SB_DQ[39]
AP22 MEM_MB_DQS_H5
AR32 MEM_MB_DQS_L5
AN32 MEM_MB_DM5
MEM_MB_DQS_H5 15,16
MEM_MB_DQS_L5 15,16
MEM_MB_DM5 15,16
AT32 MEM_MB_DATA40
AP31 MEM_MB_DATA41
AR33 MEM_MB_DATA42
AM32 MEM_MB_DATA43
AT31 MEM_MB_DATA44
AR31 MEM_MB_DATA45
SB_DQ[40]
SB_DQ[41]
SB_DQ[42]
SB_DQ[43]
SB_DQ[44]
SB_DQ[45]
SB_DQ[46]
SB_DQ[47]
AR36 MEM_MB_DQS_H6
AR37 MEM_MB_DQS_L6
AM33 MEM_MB_DM6
MEM_MB_DQS_H6 15,16
MEM_MB_DQS_L6 15,16
MEM_MB_DM6 15,16
AR35 MEM_MB_DATA48
AT36 MEM_MB_DATA49
AN33 MEM_MB_DATA50
AP36 MEM_MB_DATA51
AP34 MEM_MB_DATA52
AT35 MEM_MB_DATA53
AN34 MEM_MB_DATA54
AP37 MEM_MB_DATA55
SB_DQ[48]
SB_DQ[49]
SB_DQ[50]
SB_DQ[51]
SB_DQ[52]
SB_DQ[53]
SB_DQ[54]
SB_DQ[55]
AL37 MEM_MB_DQS_H7
AM36 MEM_MB_DQS_L7
AK35 MEM_MB_DM7
MEM_MB_DQS_H7 15,16
MEM_MB_DQS_L7 15,16
MEM_MB_DM7 15,16
AL35 MEM_MB_DATA56
AM35 MEM_MB_DATA57
AJ36 MEM_MB_DATA58
AJ37 MEM_MB_DATA59
AN35 MEM_MB_DATA60
AM34 MEM_MB_DATA61
AJ35 MEM_MB_DATA62
AL36 MEM_MB_DATA63
SB_DQ[56]
SB_DQ[57]
SB_DQ[58]
SB_DQ[59]
SB_DQ[60]
SB_DQ[61]
SB_DQ[62]
SB_DQ[63]

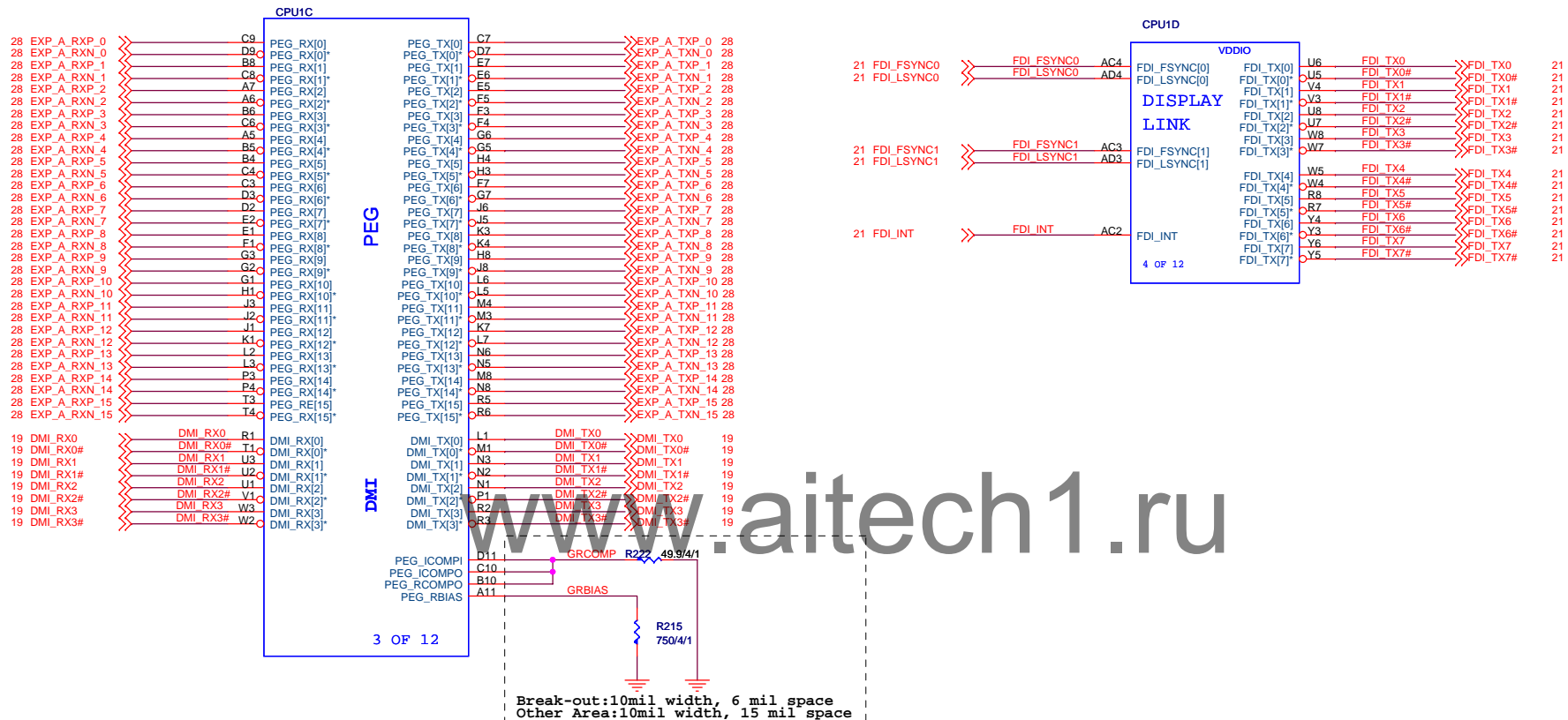


MICRO-STAR INT'L CO.,LTD

MS-7613

Size Custom Document Description CPU-Memory CH-B Rev 10

Date: Tuesday, July 21, 2009 Sheet 8 of 53

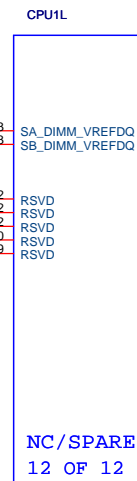
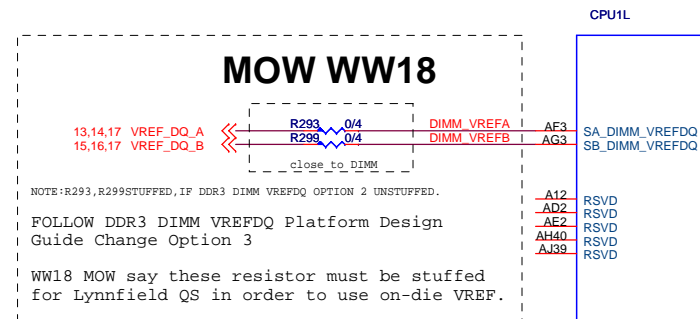
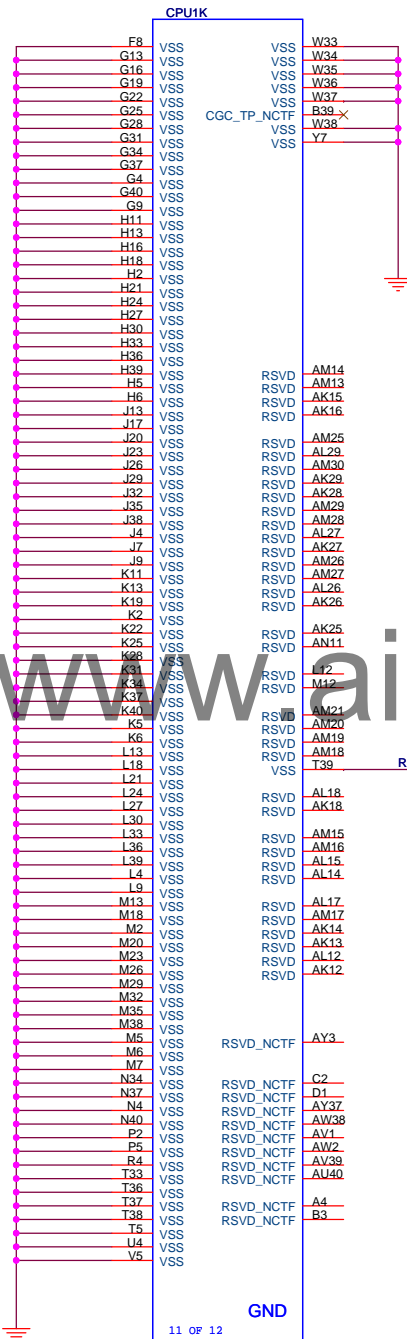
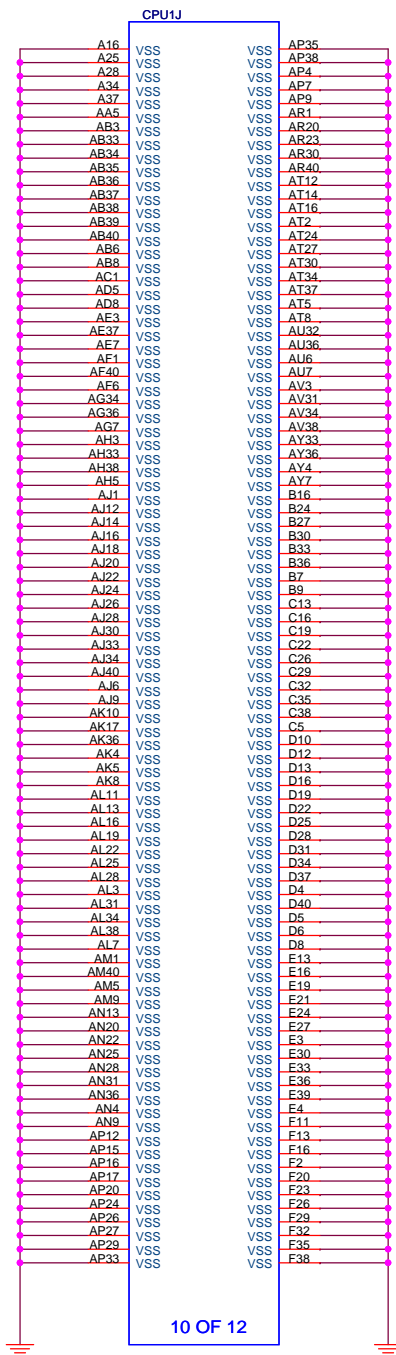


MICRO-STAR INT'L CO.,LTD

MS-7613

Size	Document Description	Rev
Custom	CPU-PEG/DMI	10
Date: Tuesday, July 21, 2009	Sheet 9 of 53	



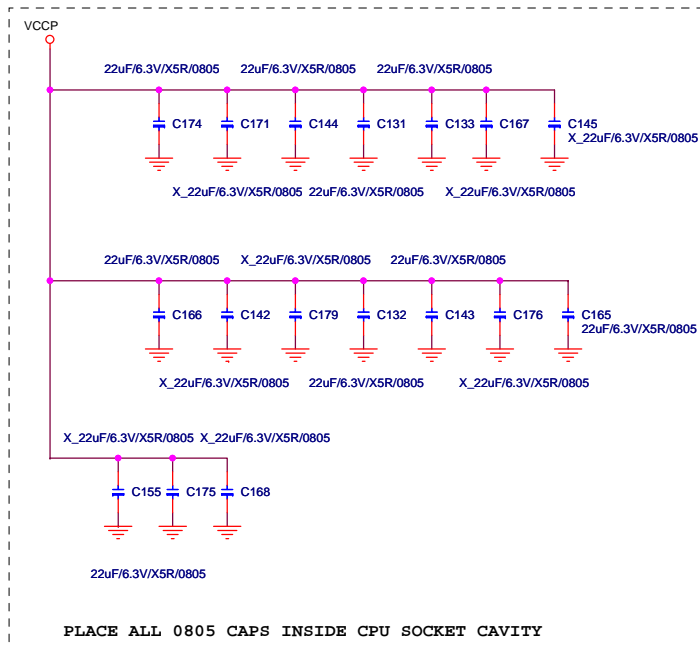


www.aitech1.ru

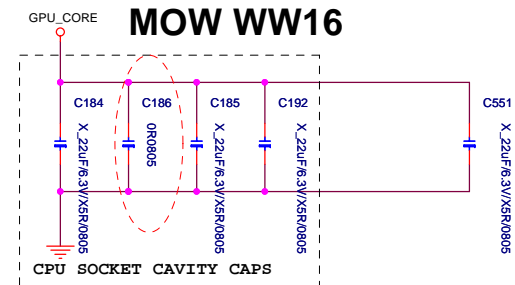


MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size Custom	Document Description CPU-GND	Rev 10
Date: Tuesday, July 21, 2009		
Sheet 11 of 53		

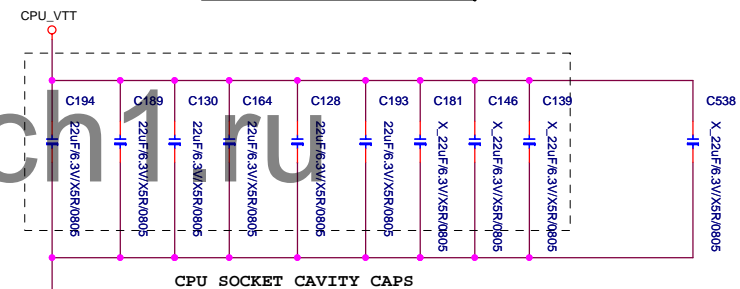
+CPU_VCCP-Decoupling



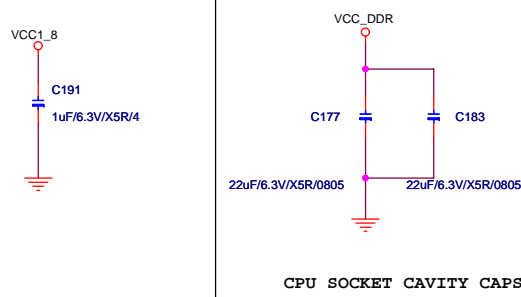
+CPU_GFX Decoupling



+CPU_VTT Decoupling



+1.5V_DDR3-Decoupling

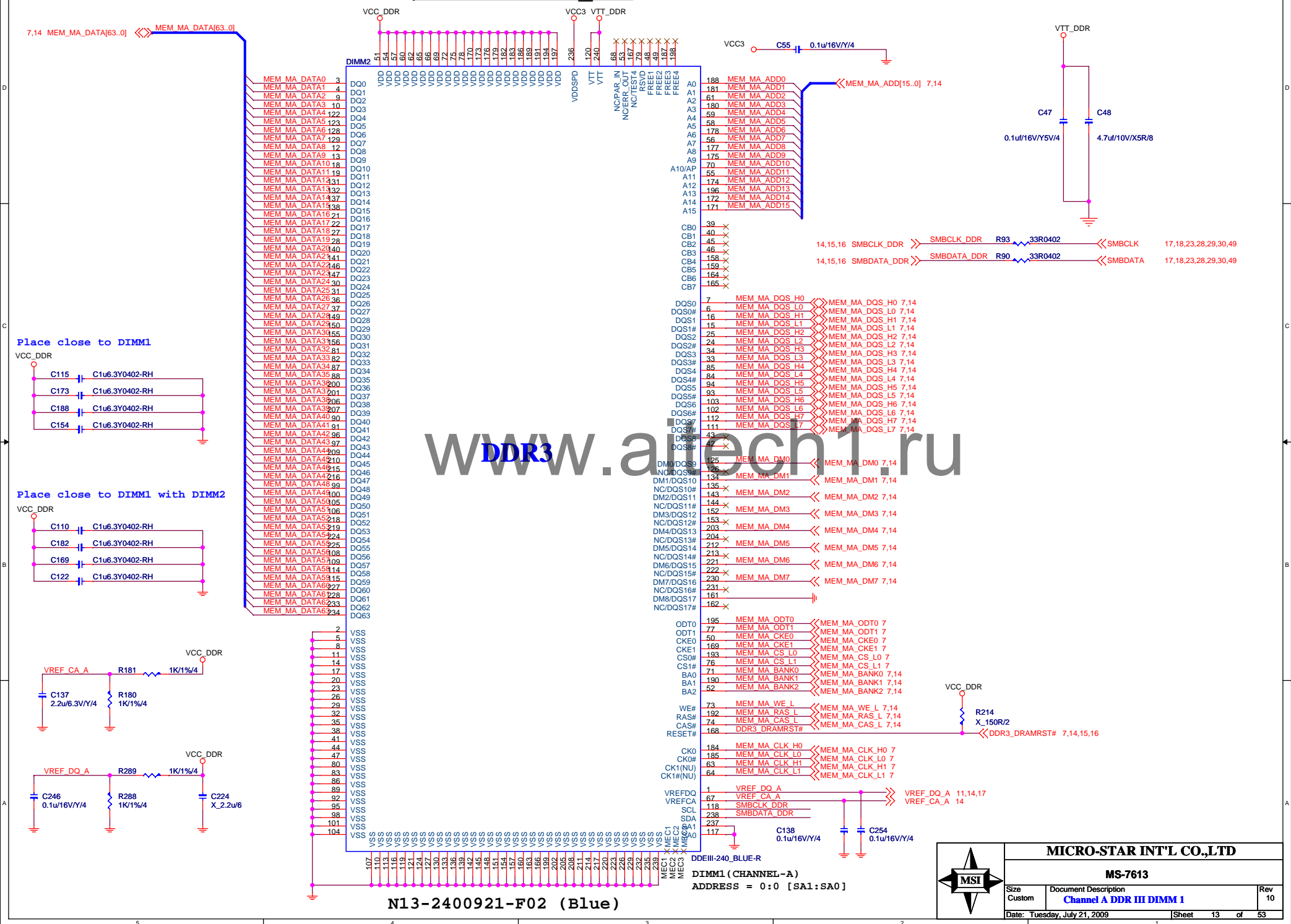


MICRO-STAR INT'L CO.,LTD

MS-7613

Size	Document Description	Rev
Custom	CPU-Decoupling	10
Date:	Tuesday, July 21, 2009	Sheet 12 of 53

DDRIII DIMM A1

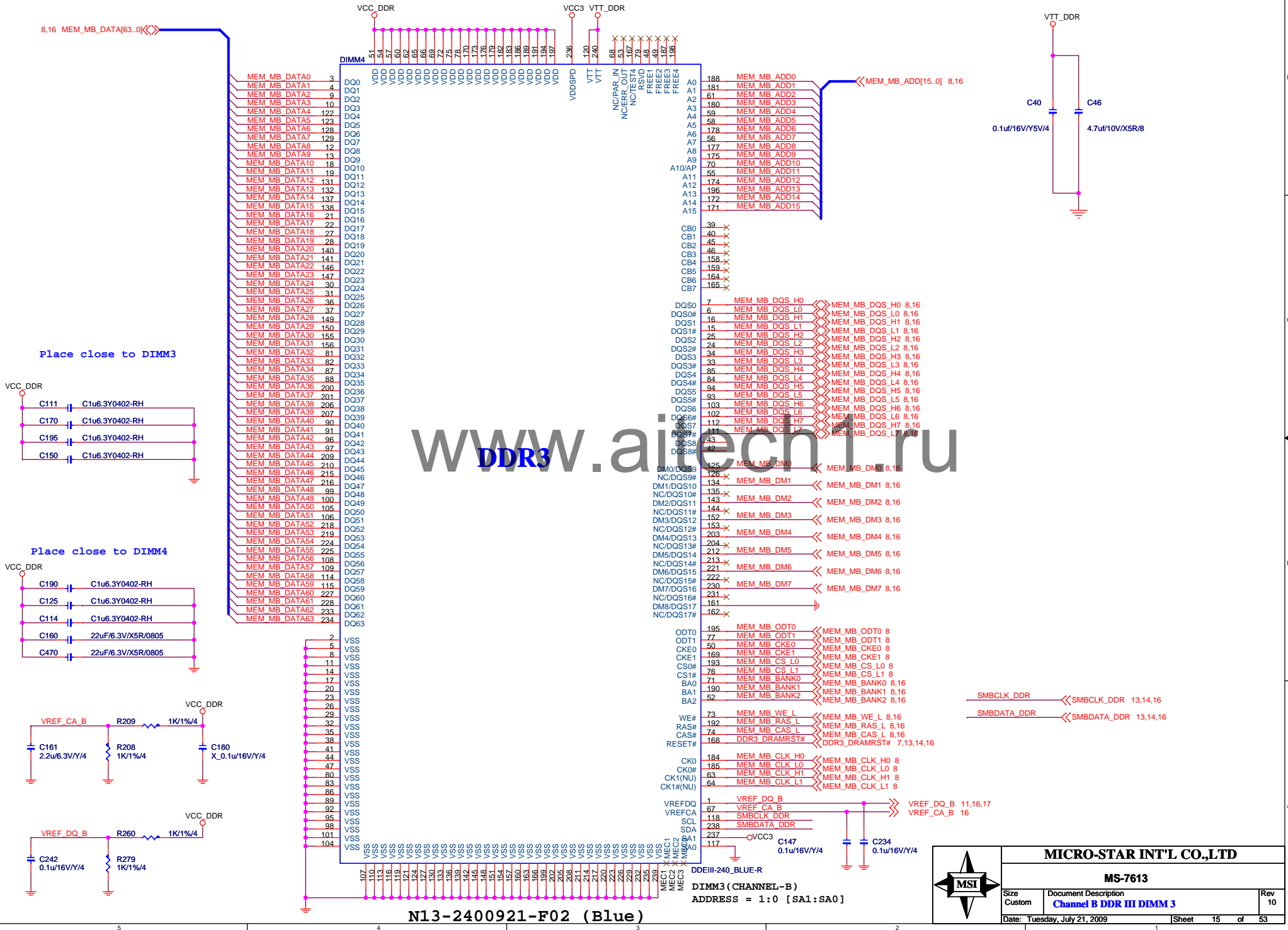


www.altech.ru



MICRO-STAR INT'L CO.,LTD			
MS-7613			
Size Custom	Document Description Channel A DDR III DIMM 2		Rev 10
Date: Tuesday, July 21, 2009		Sheet	14 of 53

DDRIII DIMM_B1



DDRIII DIMM_B2

8,15 MEM_MB_DATA[63:0]

VCC_DDR VCC3 VTT_DDR



www.aitech1.ru

DDR3

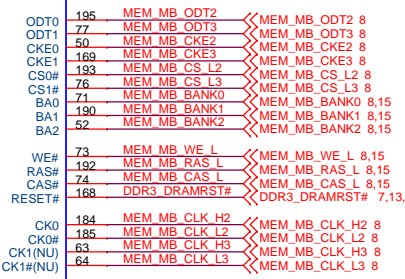
VTT_DDR

C51

C49

0.1uF/16V/Y5V4

4.7uF/10V/X5R/8



SMBCLK_DDR SMBCLK_DDR 13,14,15
SMBDATA_DDR SMBDATA_DDR 13,14,15

N13-2400601-F02 (Black)

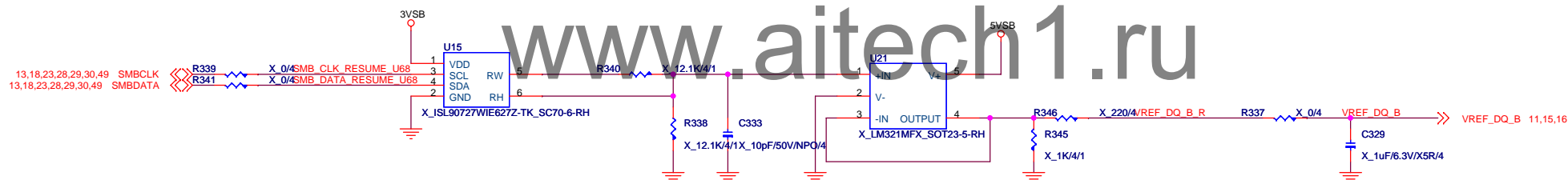
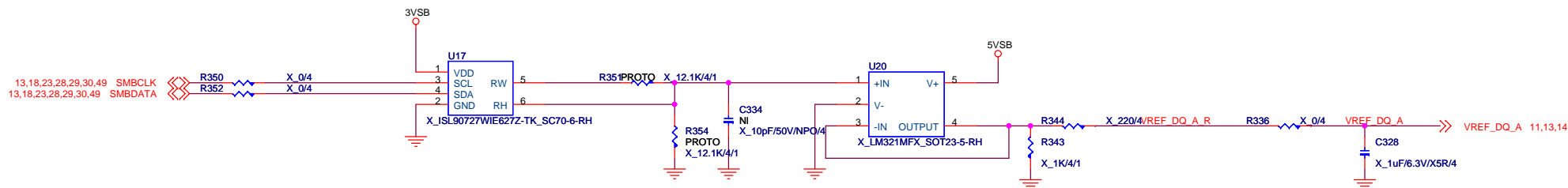
DDEIII-240_BLACK-R
DIMM4 (CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]



MICRO-STAR INT'L CO.,LTD

MS-7613

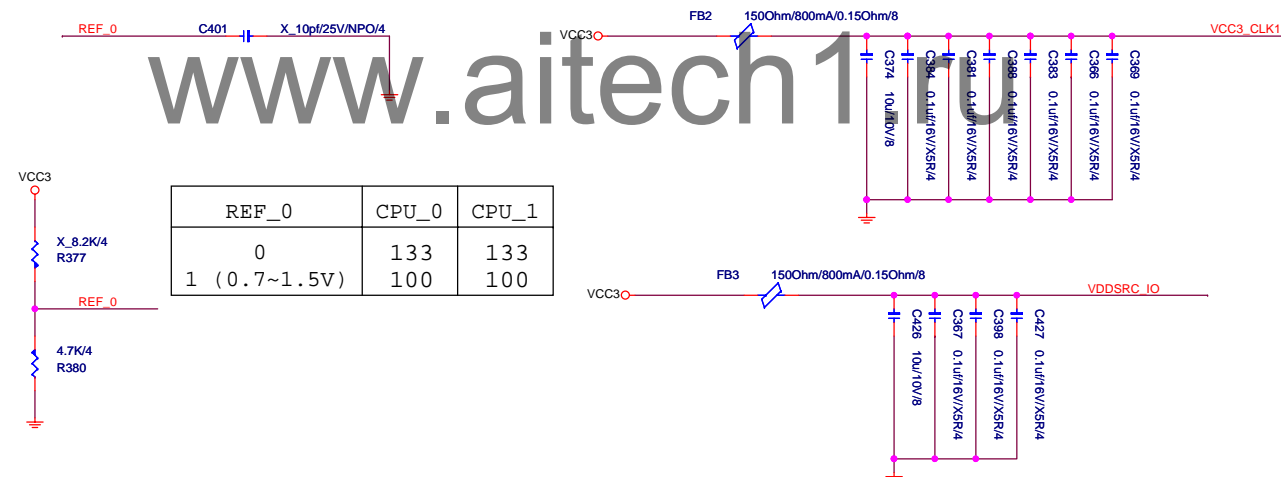
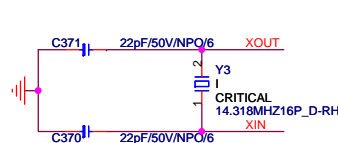
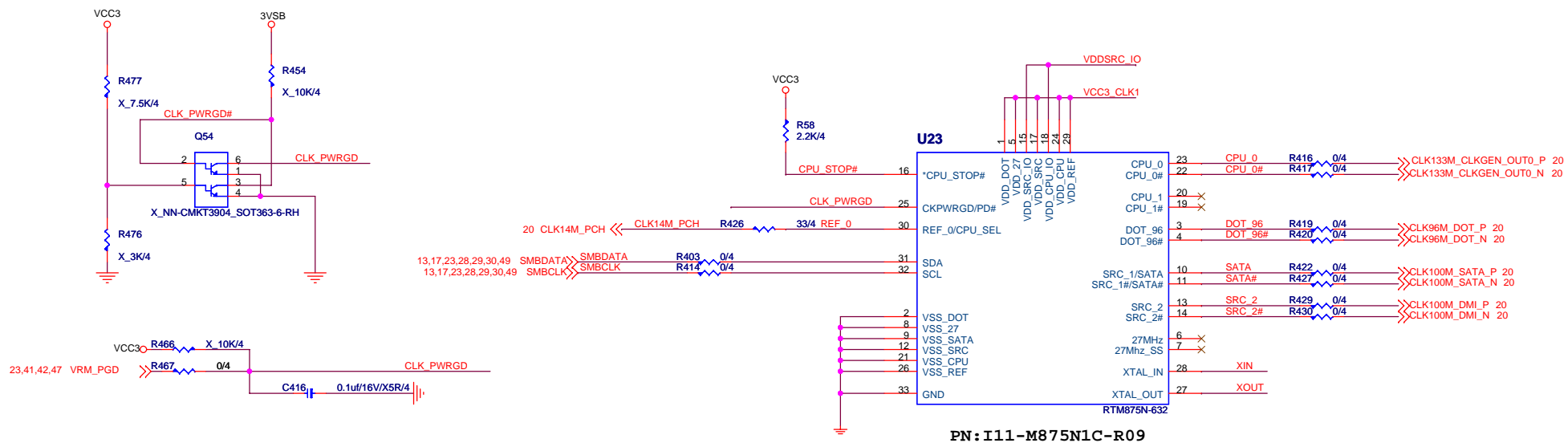
Size	Document Description	Rev
Custom	Channel B DDR III DIMM 4	10
Date: Tuesday, July 21, 2009	Sheet 16 of 53	



MICRO-STAR INT'L CO.,LTD

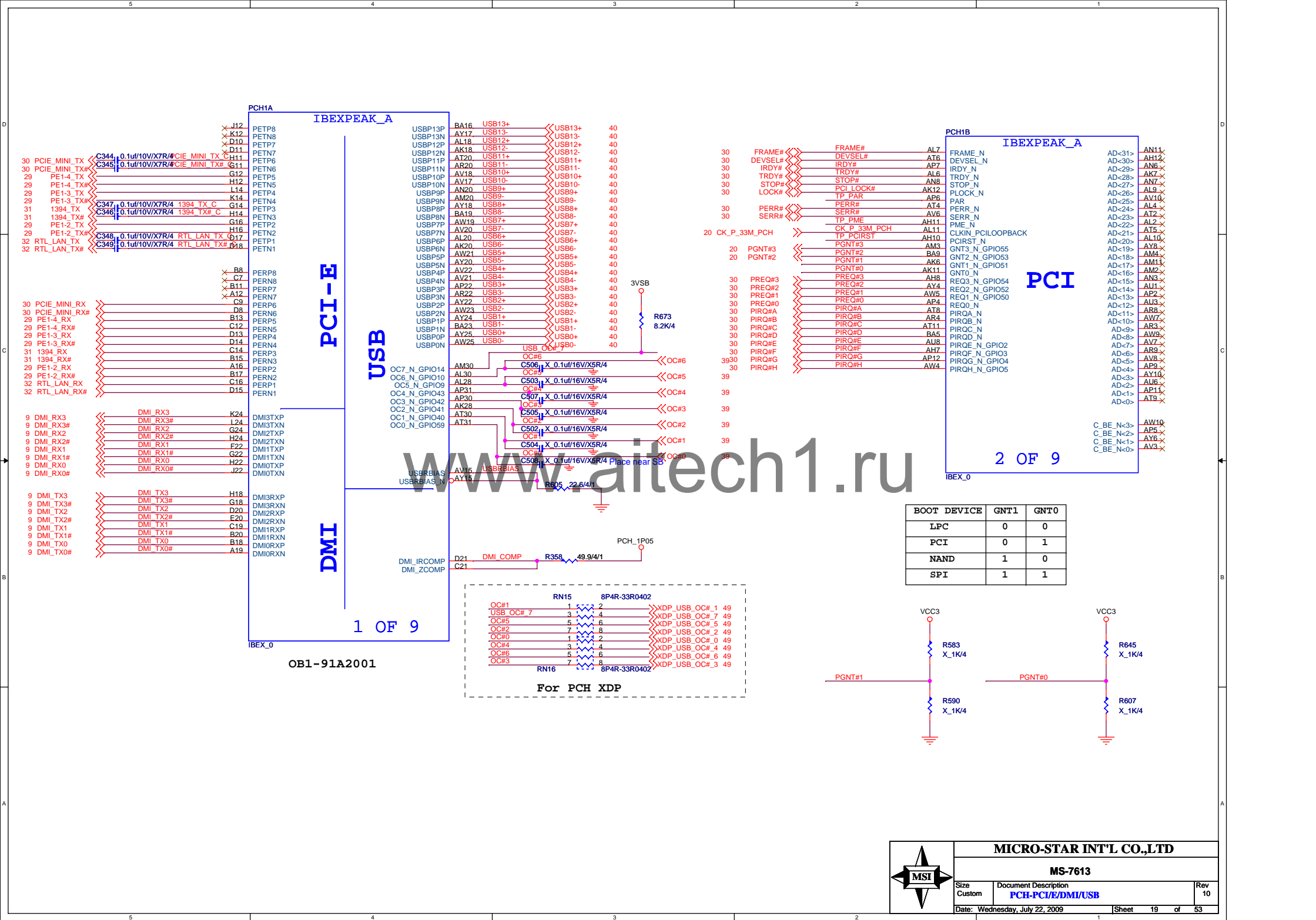
MS-7613

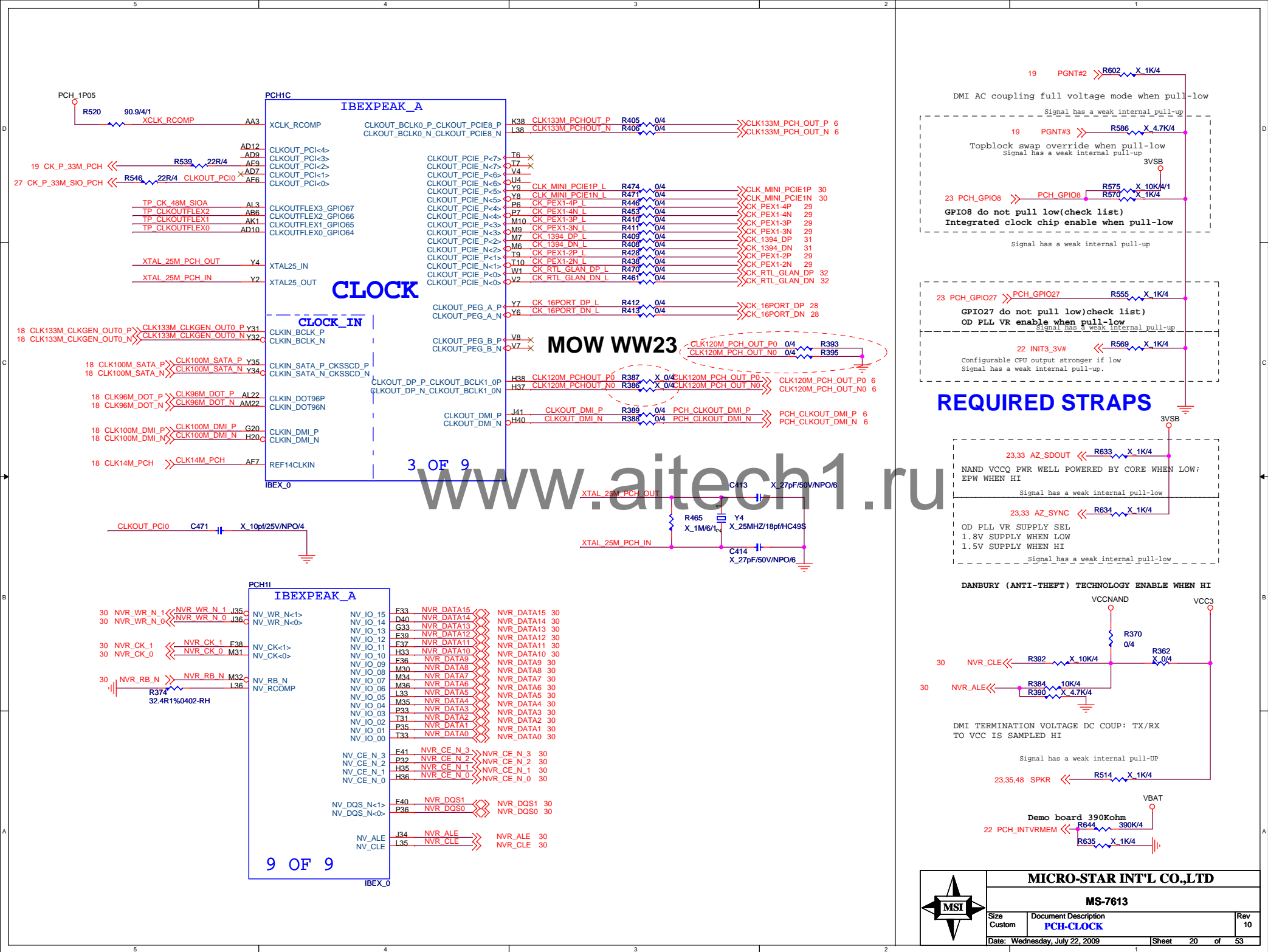
Size Custom	Document Description DIMM VREF (Option)	Rev 10
Date: Tuesday, July 21, 2009		Sheet 17 of 53

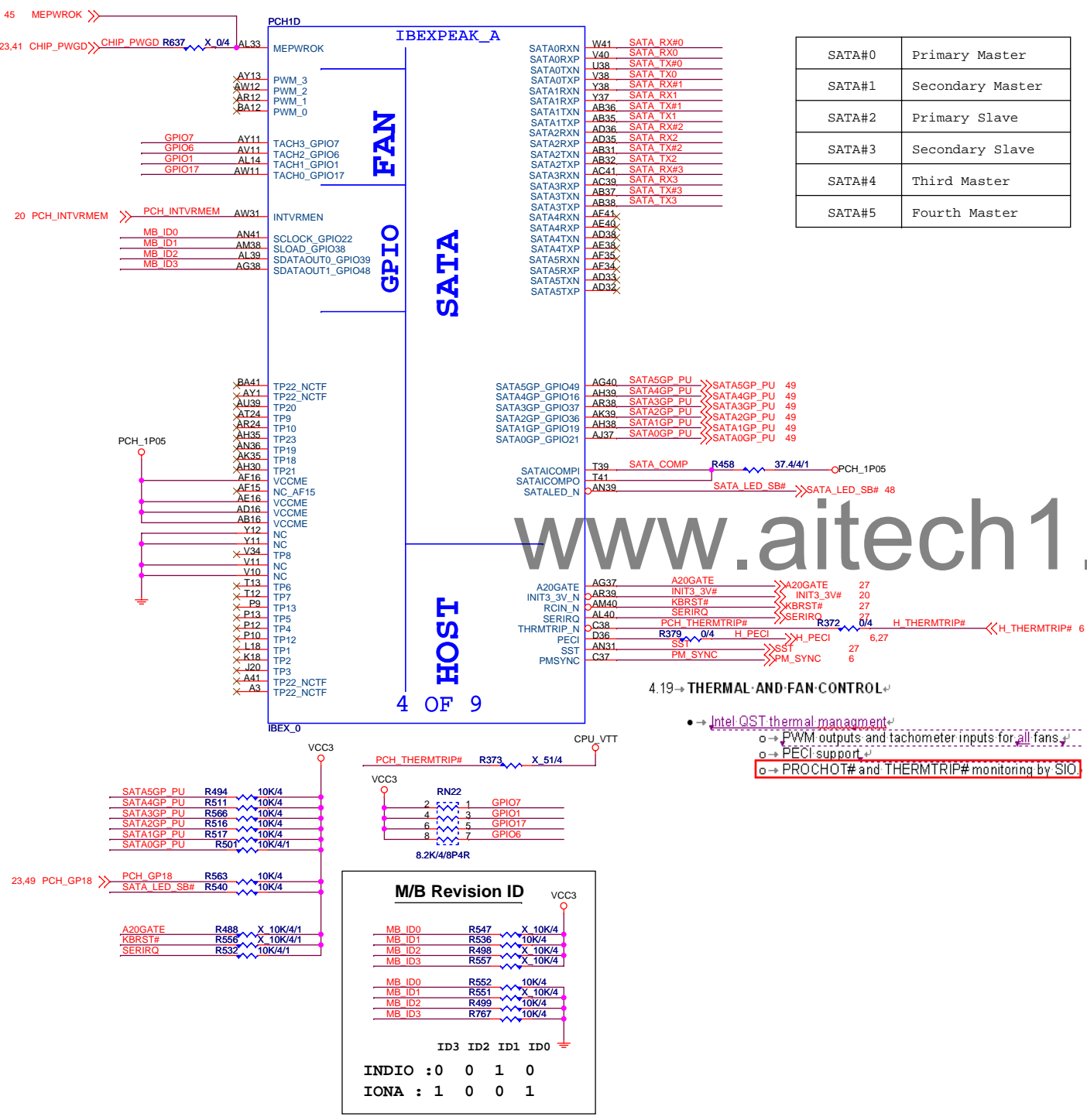


REF_0	CPU_0	CPU_1
0	133	133
1 (0.7~1.5V)	100	100



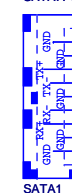






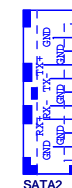
SATA connector

SATA7PSM_BLUE-P-RH-2



Dark Blue
N5N-07M1081-F02

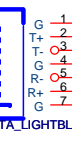
SATA7PSM_WHITE-P-RH-2



White
N5N-07M1091-F02

SATA3

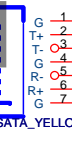
CONN-SATA_LIGHTBLUE



Light Blue
N5N-07M0581-F02

SATA4

CONN-SATA_YELLOW



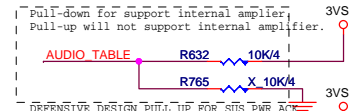
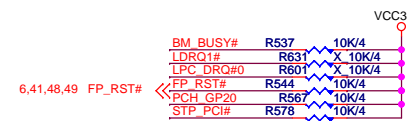
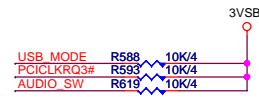
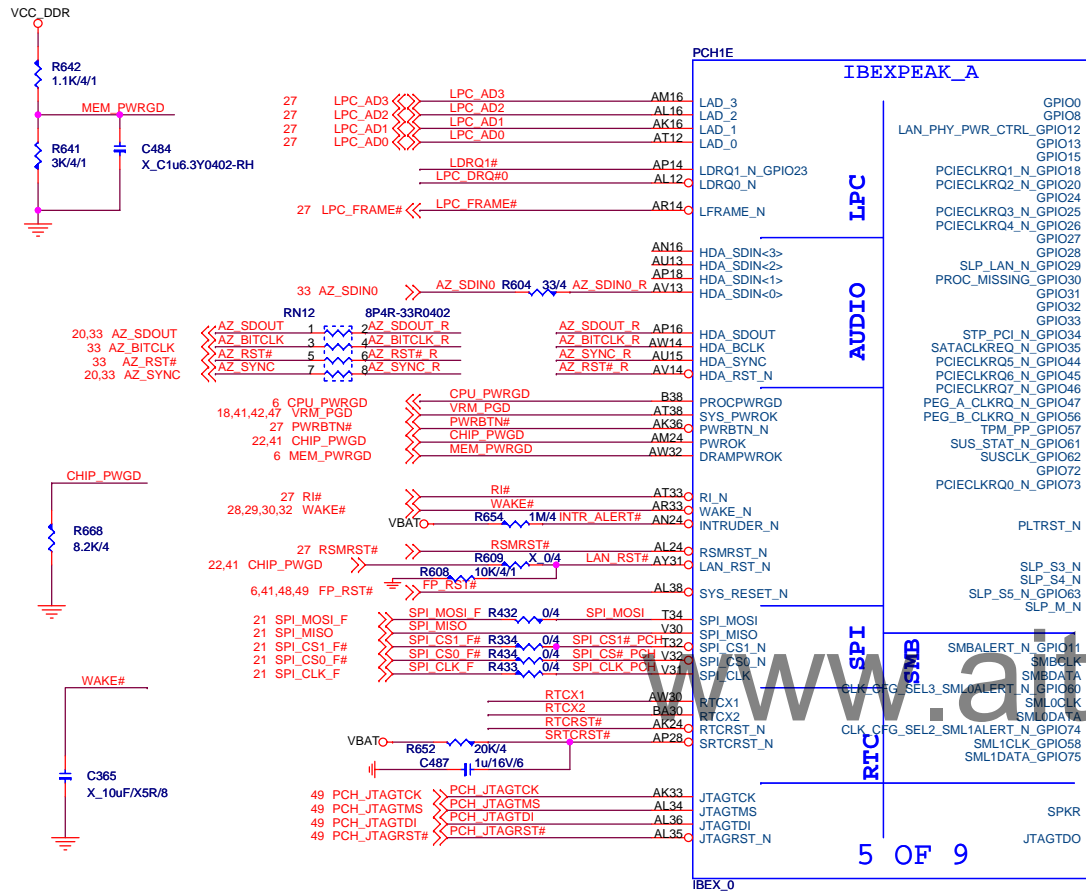
Yellow
N5N-07M0661-F02



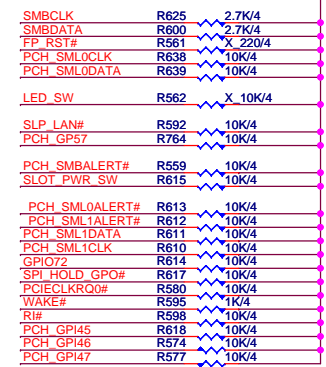
MICRO-STAR INT'L CO.,LTD

MS-7613

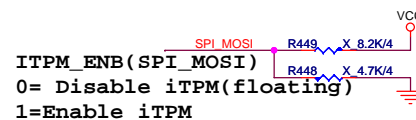
Size	Document Description	Rev
Custom	PCH-SATA/HOST/FAN/GPIO	10
Date: Wednesday, July 22, 2009	Sheet 22 of 53	



GPIO15(SPI_HOLD_GPO#) Demo board 1.0 change to high
 TLS CONFIDENTIALITY DISABLE WHEN LOW



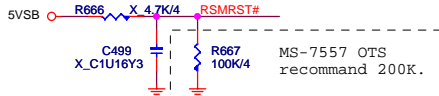
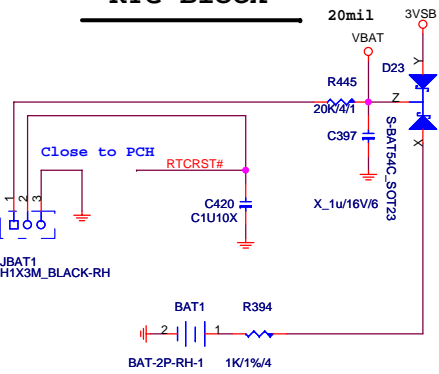
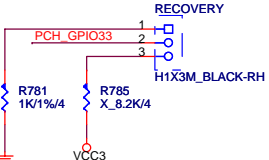
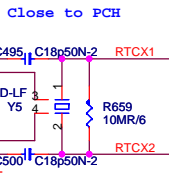
Disable ME in Manufacturing Mode
 (GPIO33 Pull Down 1K)



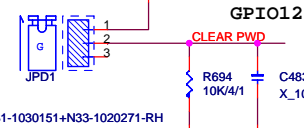
CMOS CLEAR JUMPER	
1 - 2	Normal
2 - 3	Clear CMOS

RTC Block

RECOVERY JUMPER	
1 - 2	ENABLE
2 - 3	DISABLE



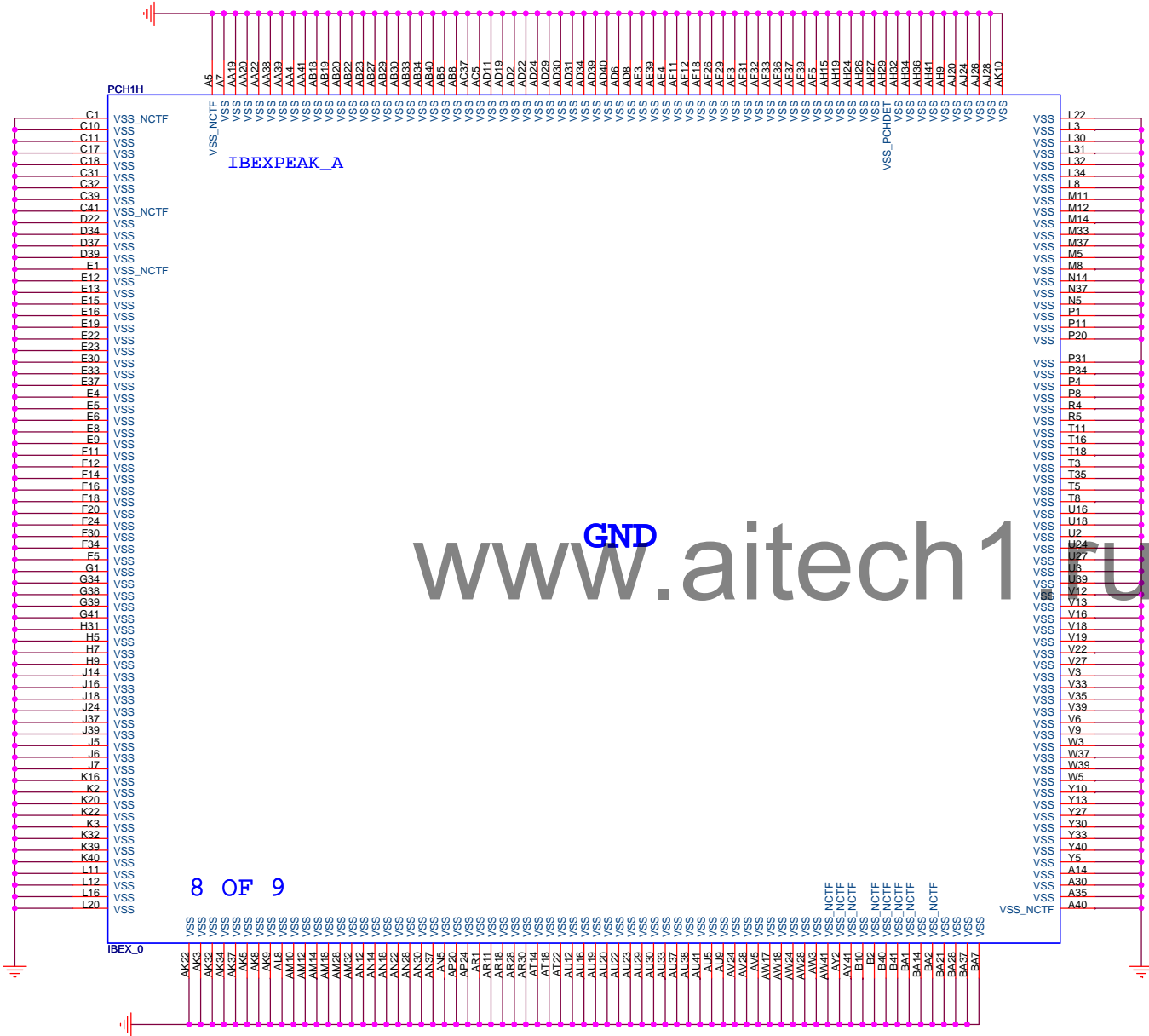
Password CLEAR JUMPER	
1 - 2	Normal
2 - 3	Clear PD



MICRO-STAR INT'L CO.,LTD

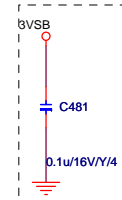
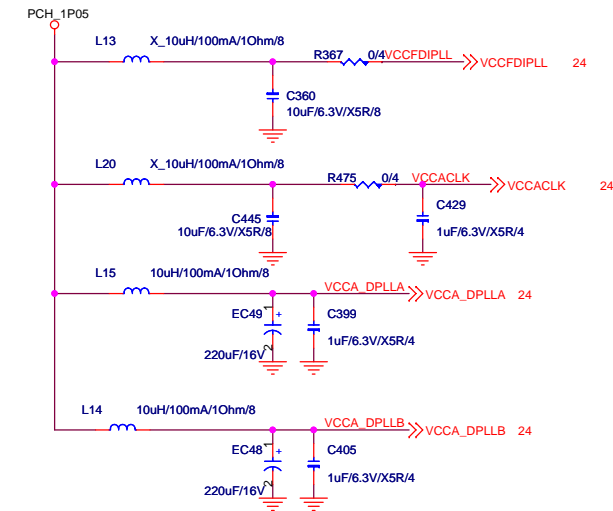
MS-7613

Size	Document Description	Rev
Custom	PCH-SMB/LPC/AUDIO/RTC	10
Date:	Wednesday, July 22, 2009	Sheet 23 of 53

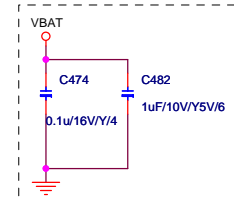


MICRO-STAR INT'L CO.,LTD			
MS-7613			
Size	Document Description		Rev
Custom	PCH-GND		10
Date: Wednesday, July 22, 2009		Sheet 25 of 53	

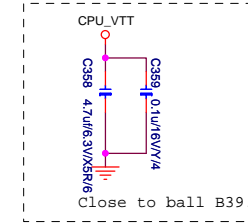
PCH decoupling cap



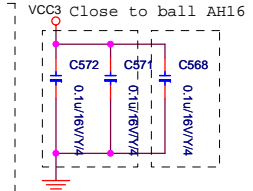
Close to ball AV25



Close to ball AY29.

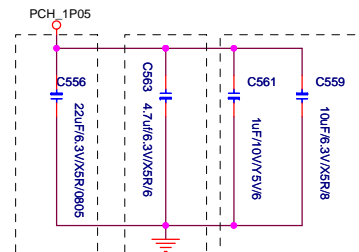


Close to ball B39.

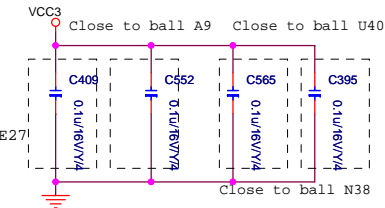


VCC3 Close to ball AH16

Close to ball AV2

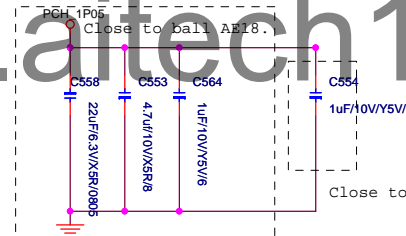
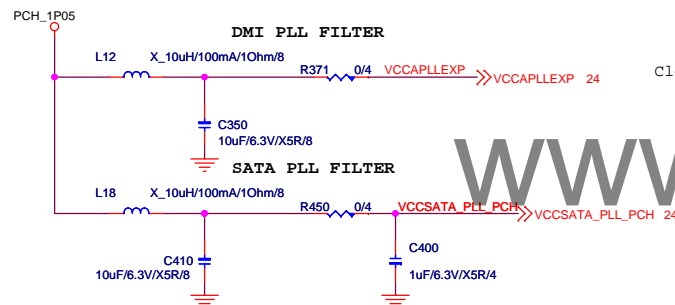


Close to ball Y26 Close to ball Y29



Close to ball AE27

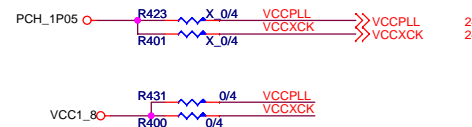
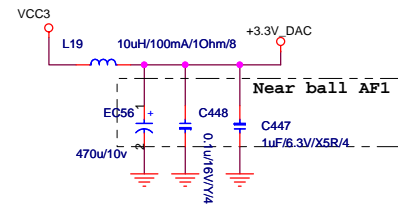
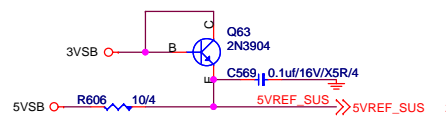
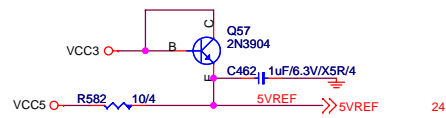
Close to ball N38



Close to ball V15

5VREF & 5VREF_SUS Sequencing Circuit

5VREF must be powered up before VCC3 or after VCC3 within 0.7V. Also, 5VREF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to 5VREF_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



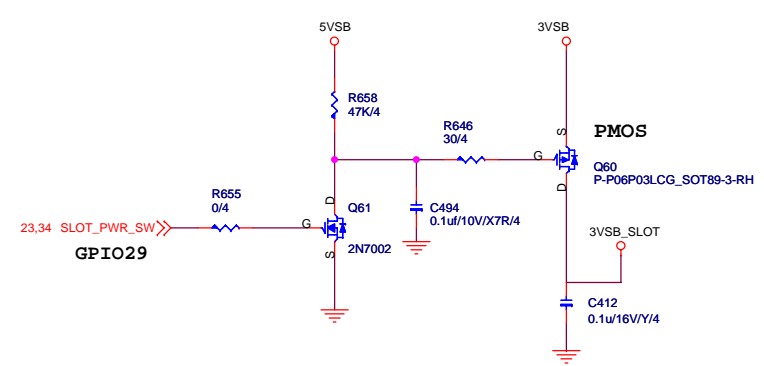
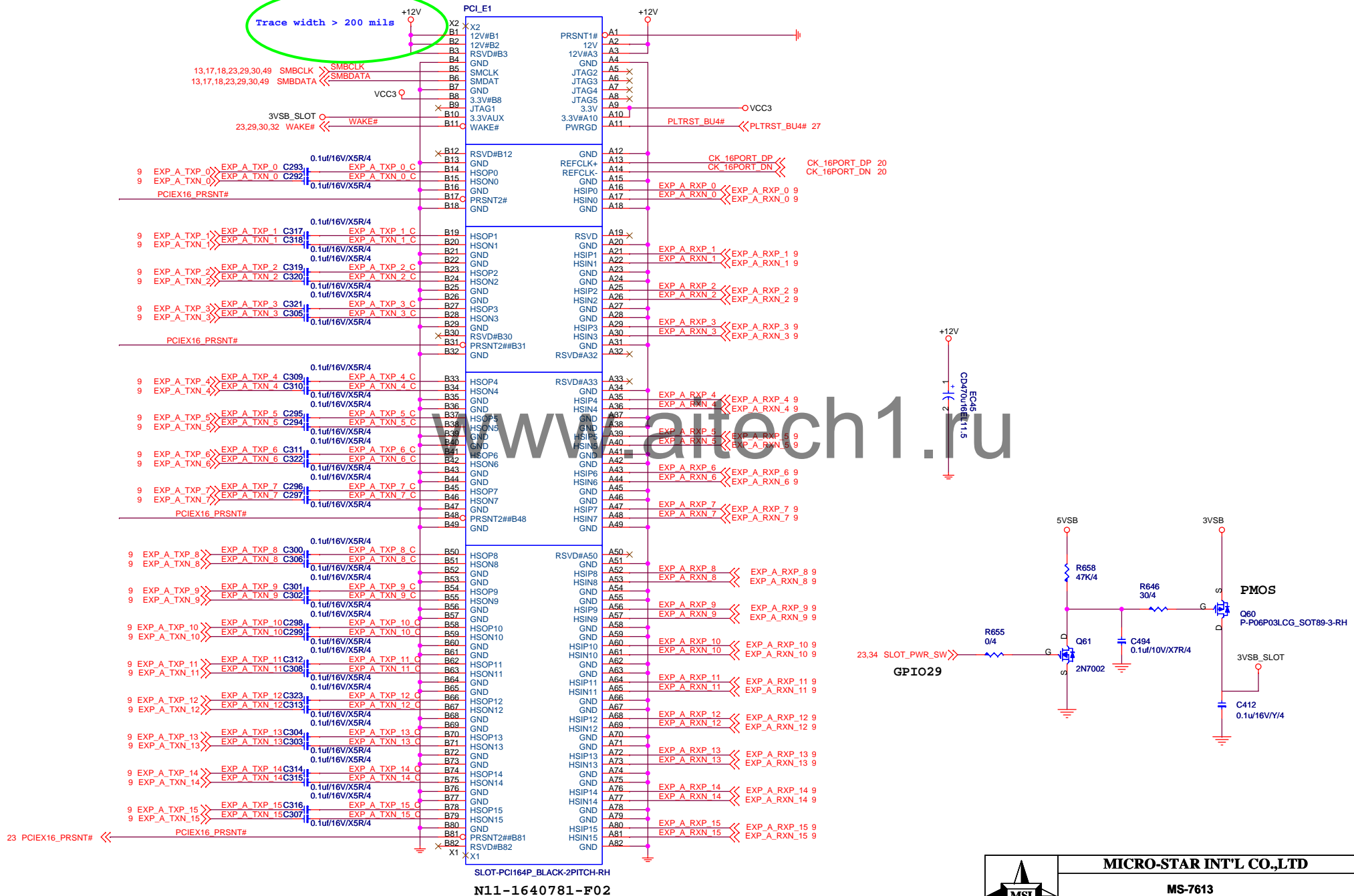
MICRO-STAR INT'L CO.,LTD

MS-7613

Size	Document Description	Rev
Custom	PCH-DECOUPLING	10
Date: Tuesday, July 21, 2009	Sheet 26 of 53	

Date: Tuesday, July 21, 2009	Sheet 27 of 53
------------------------------	----------------

PCI_Express X16 Slot



N11-1640781-F02

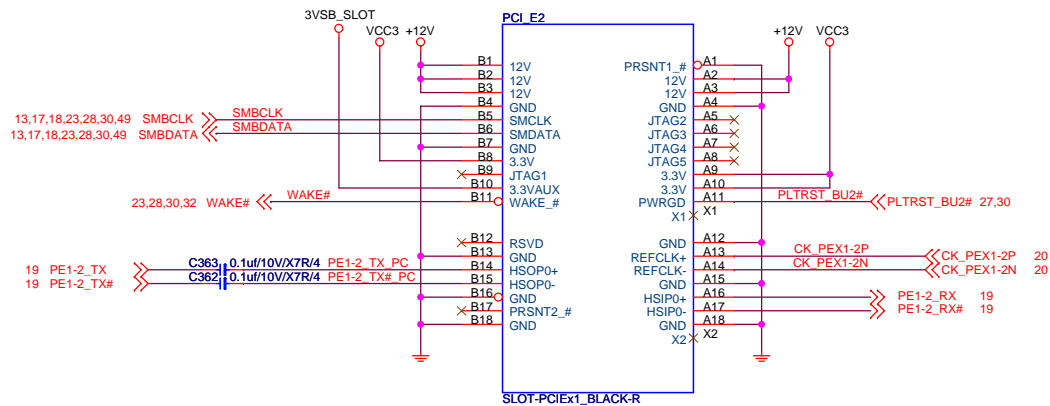


MICRO-STAR INT'L CO.,LTD

MS-7613

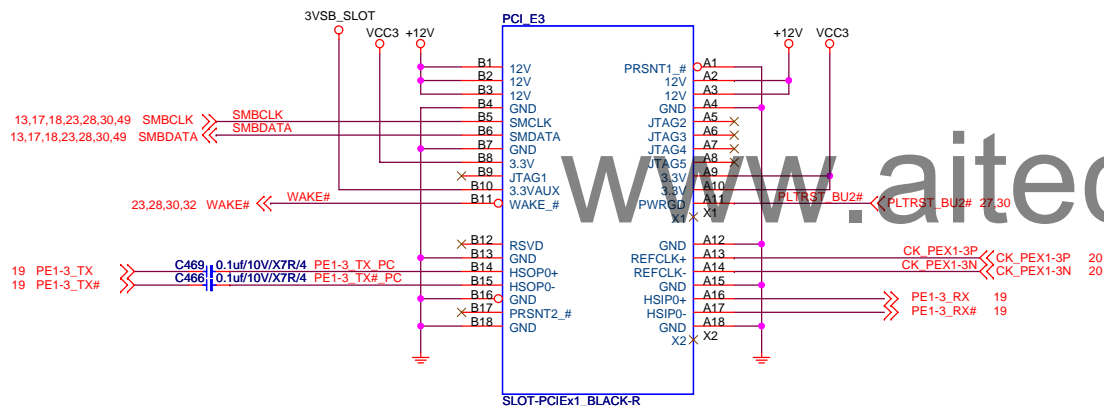
Size Custom	Document Description PCIE X16 SLOT	Rev 10
Date: Tuesday, July 21, 2009		Sheet 28 of 53

PCI EXPRESS x1-PORT1



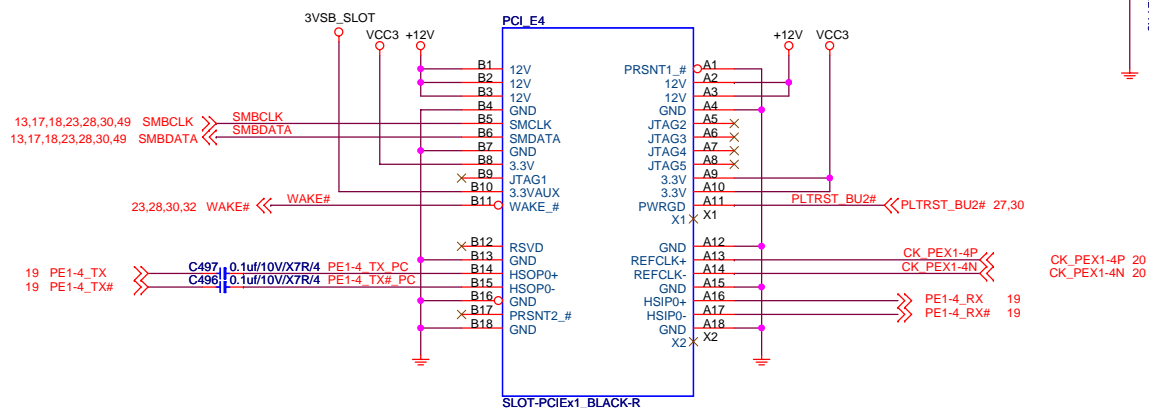
N11-0360281-K06

PCI EXPRESS x1-PORT2



N11-0360281-K06

PCI EXPRESS x1-PORT3



N11-0360281-K06

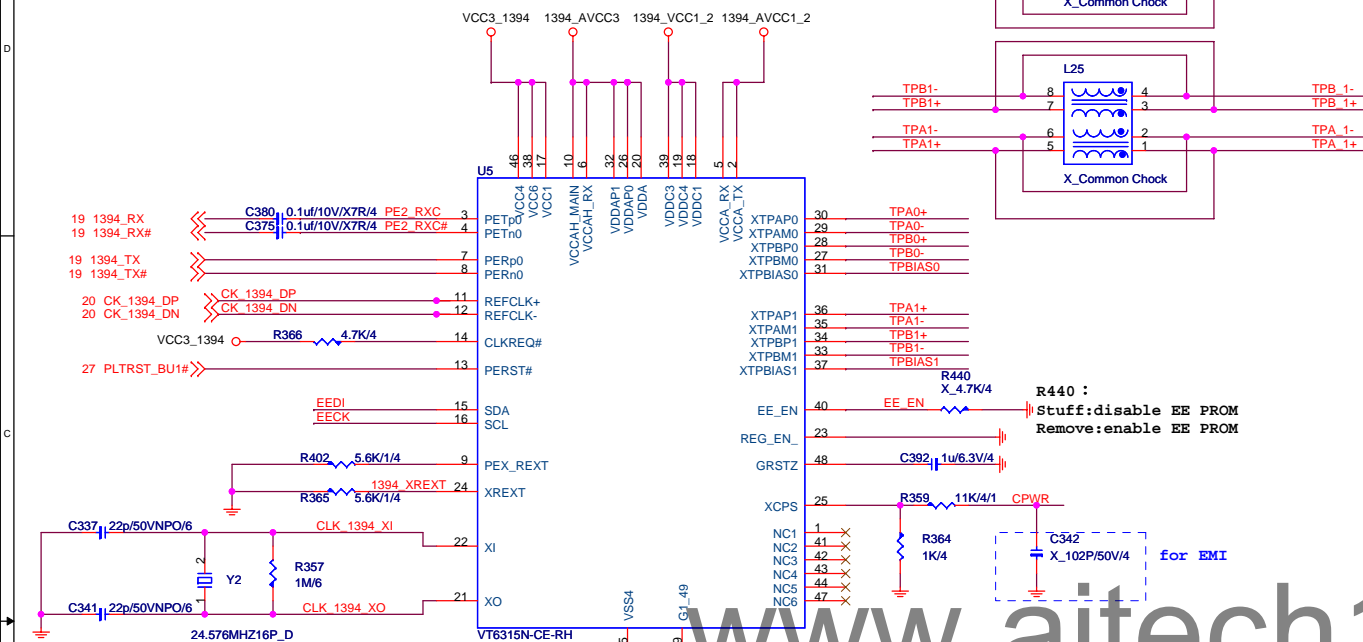


MICRO-STAR INT'L CO.,LTD

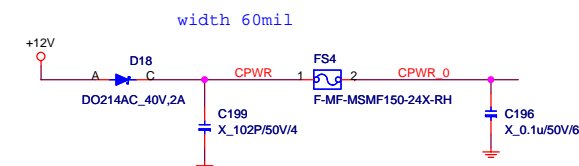
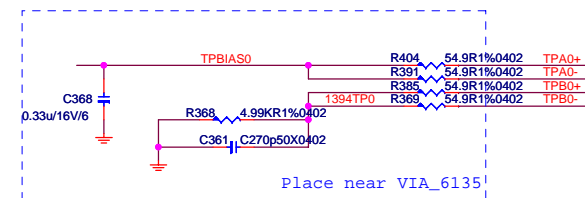
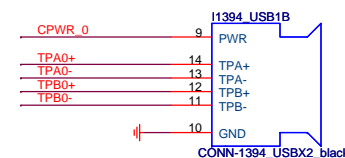
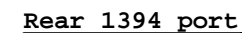
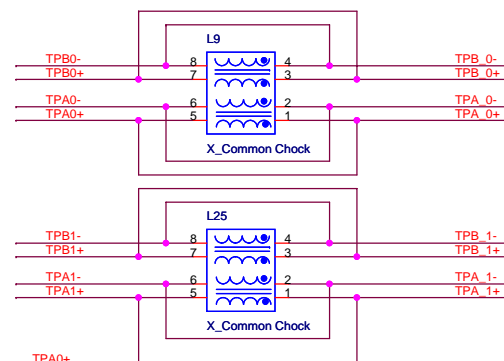
MS-7613

Size	Document Description	Rev
Custom	PCIE X1 SLOT	10
Date:	Tuesday, July 21, 2009	Sheet 29 of 53

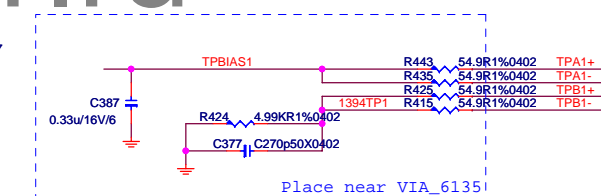
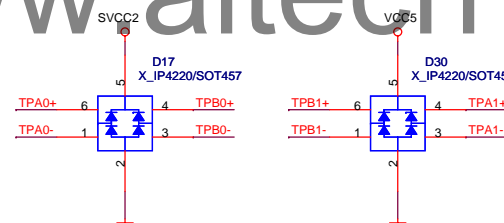
1394 CONTROLLER



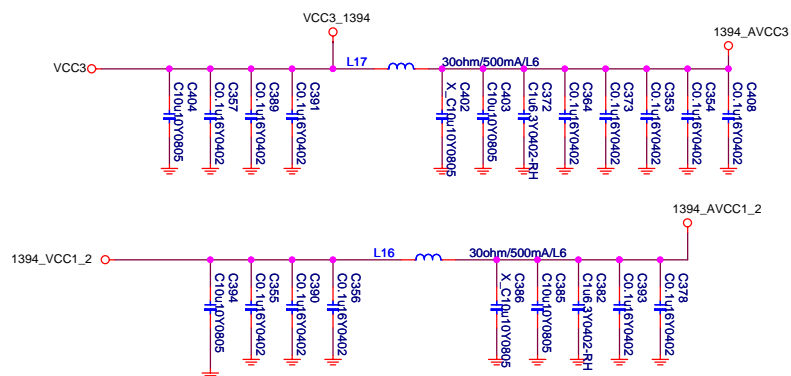
B07-6315N1C-V01



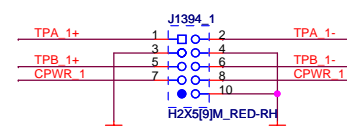
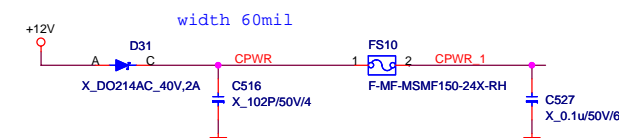
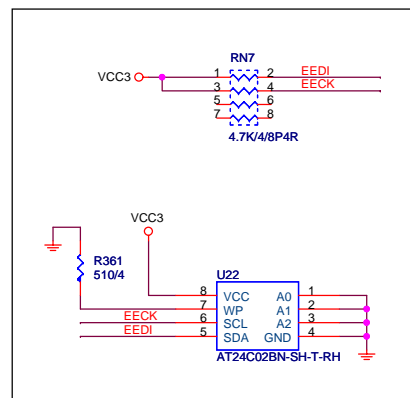
Front 1394 pin header



close to chip of all Cap.



close to chip of all Cap.

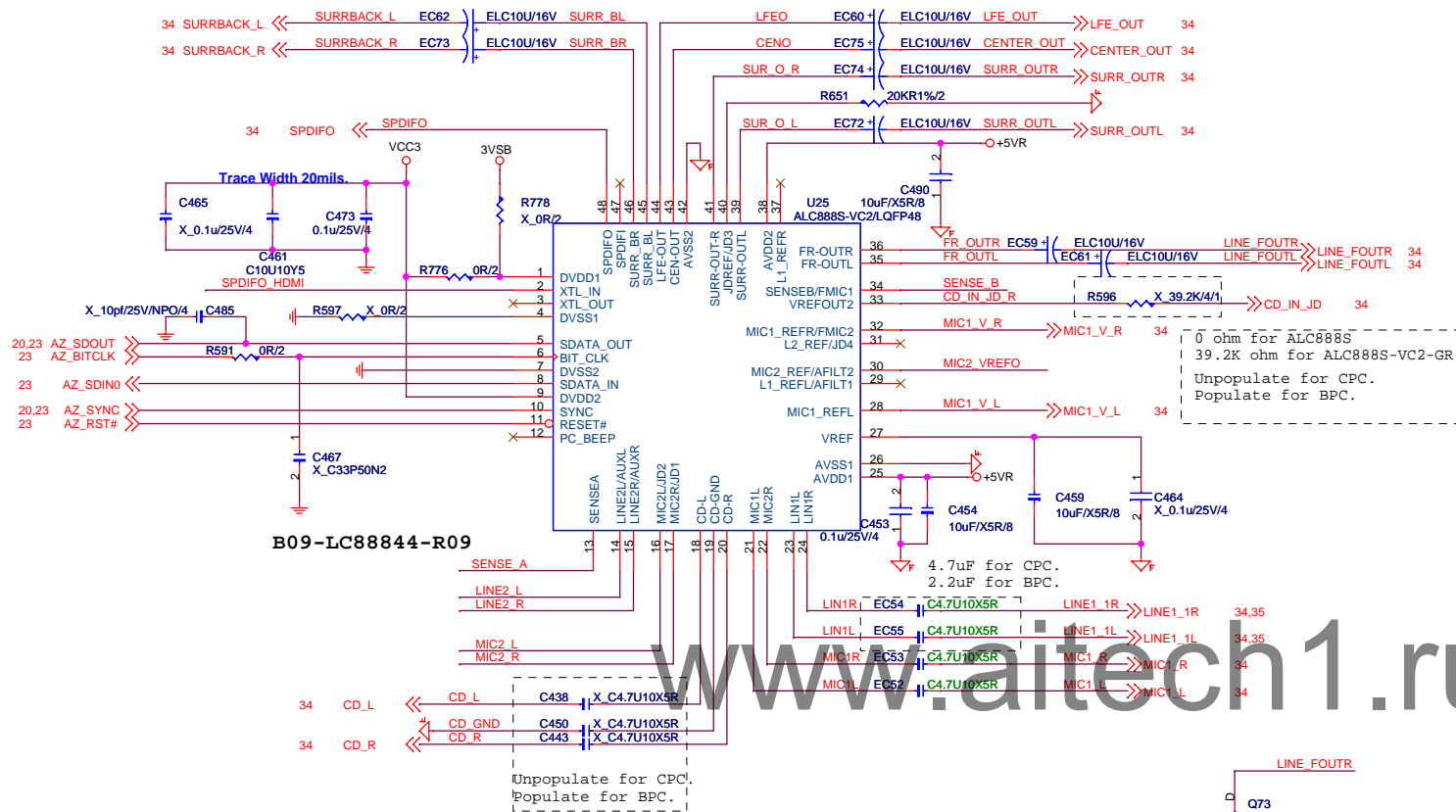


For Intel 1394 pinheader

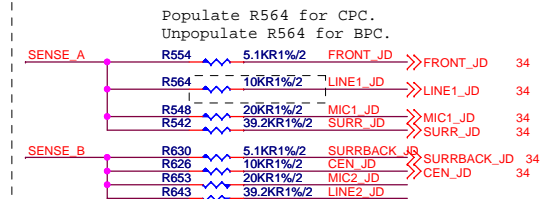


MICRO-STAR INT'L CO.,LTD			
MS-7613			
Size Custom	Document Description 1394 Controller - VT6315N-CE	Ref 1	
Date: Tuesday, July 21, 2009	Sheet 31	of 53	

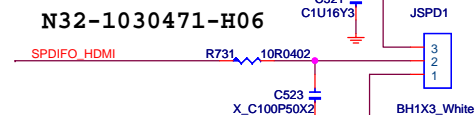
ALC888S CODEC



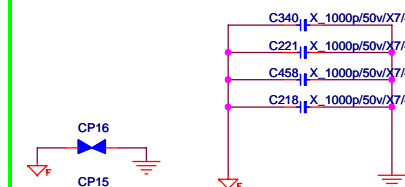
ALC888S JACK DETECT

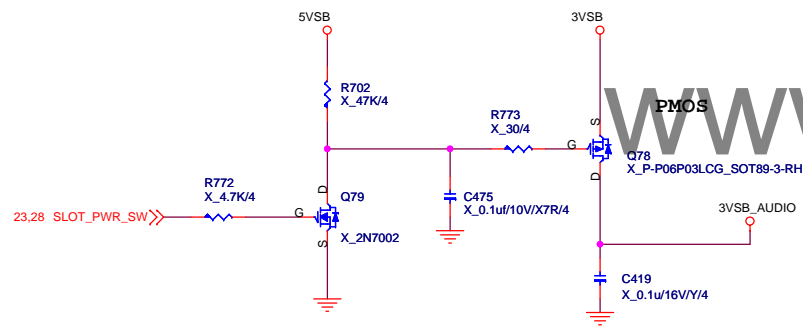
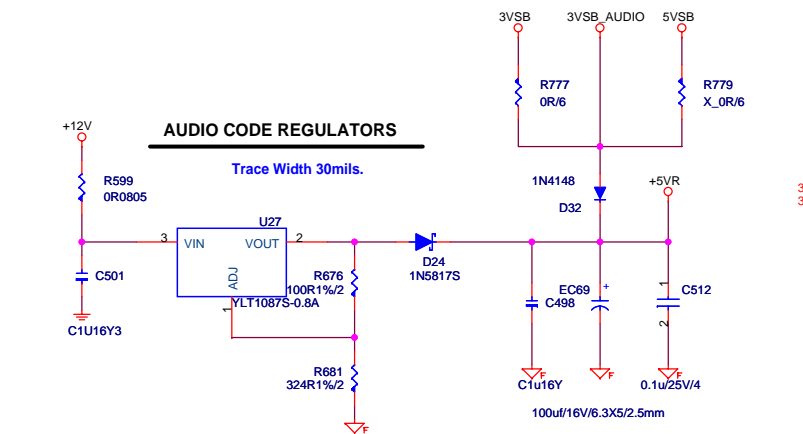


SPDIF_OUT

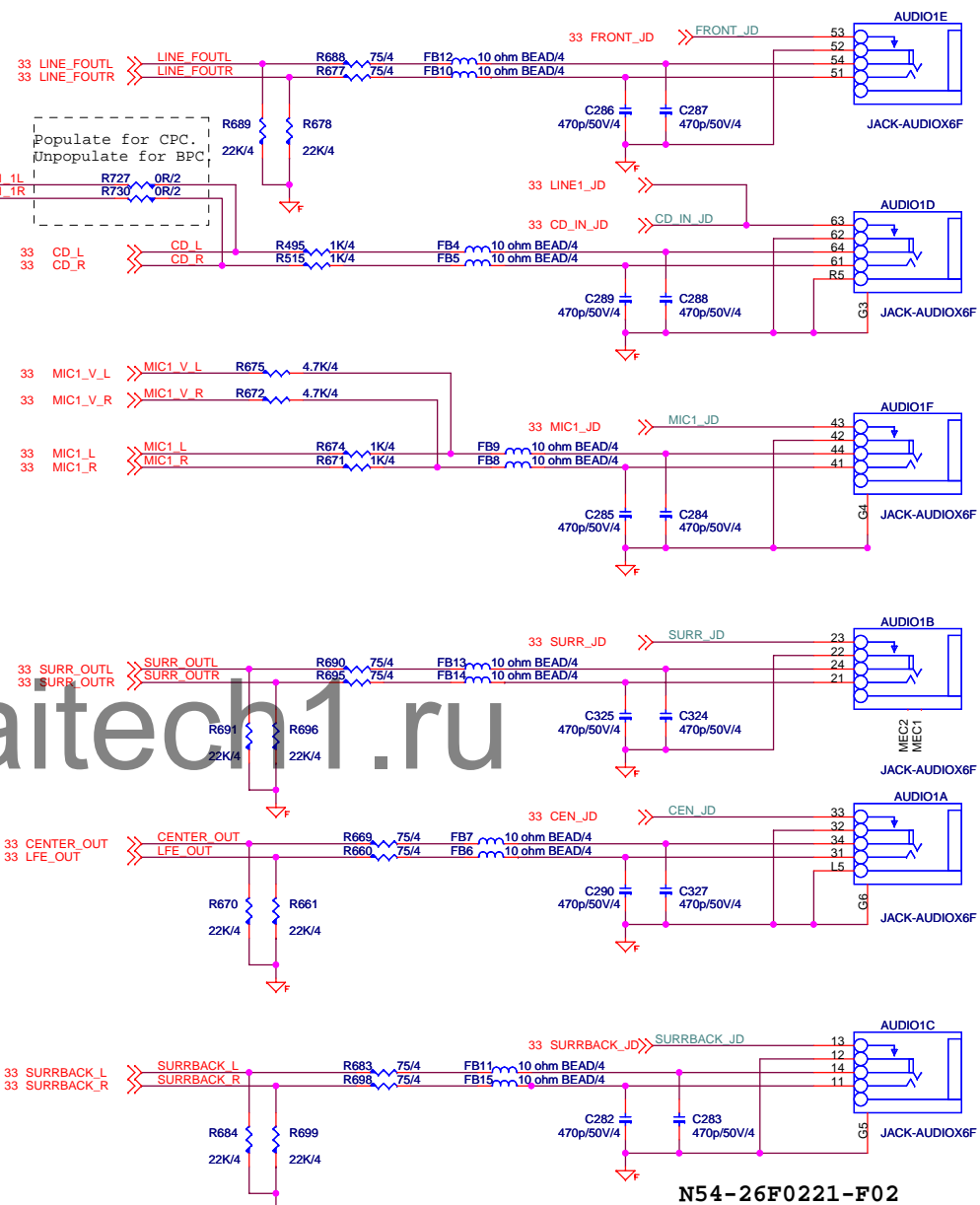
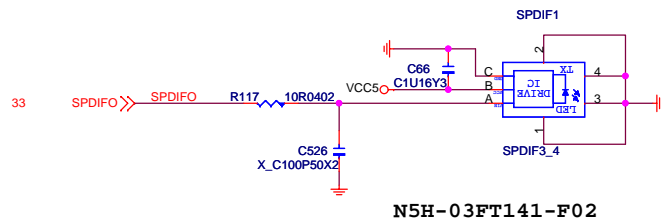


For EMI





SPDIF OUT (REAR)



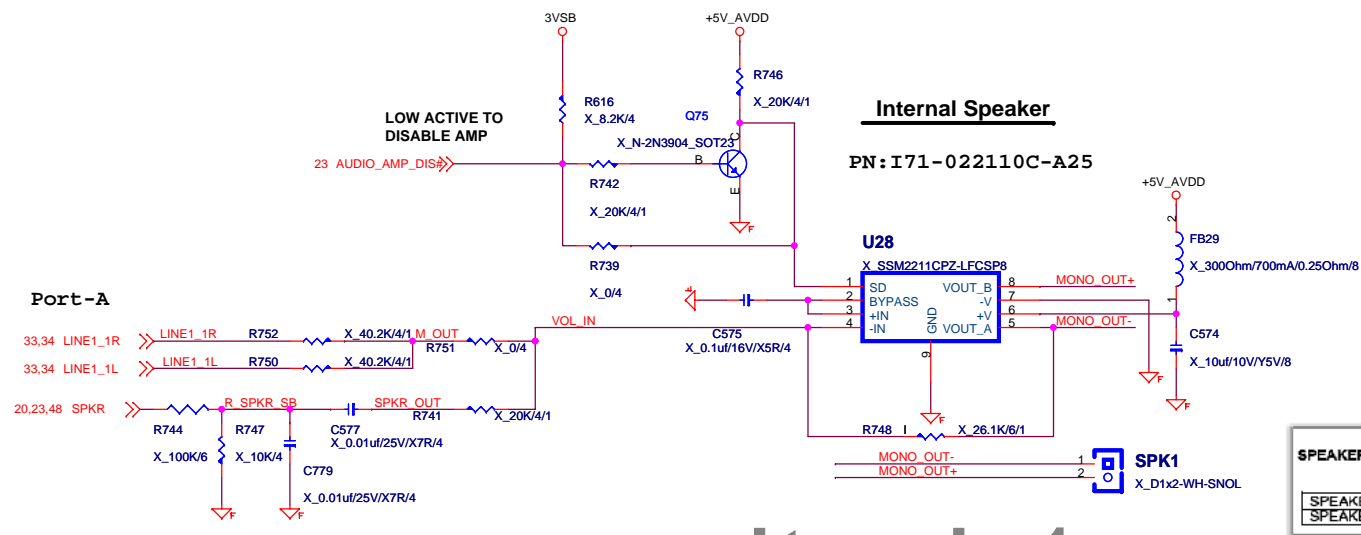
N54-26F0221-F02



MICRO-STAR INT'L CO.,LTD

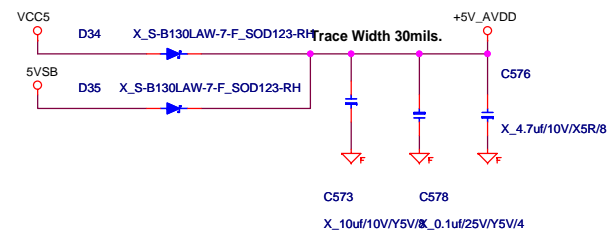
MS-7613

Size	Document Description	Rev
Custom	AUDIO JACK	10
Date:	Tuesday, July 21, 2009	Sheet 34 of 53



www.aitech1.ru

AUDIO AMPLIFIER POWER REGULATORS

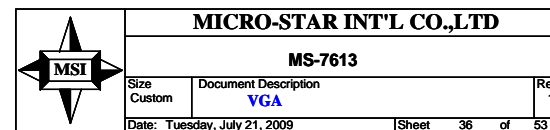


MICRO-STAR INT'L CO.,LTD

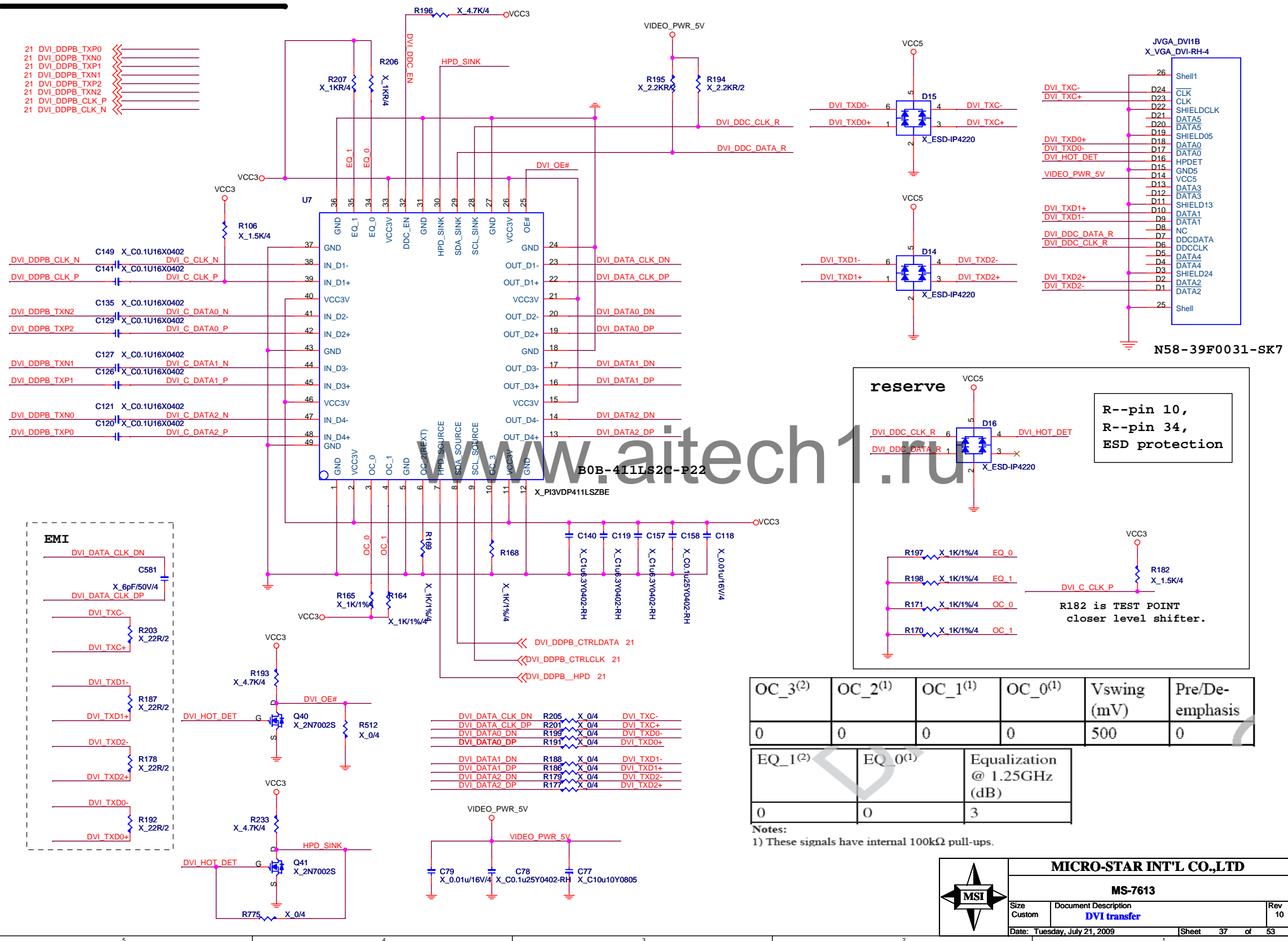
MS-7613

Size	Document Description	Rev
Custom	AUDIO AMPLIFIER	10
Date:	Tuesday, July 21, 2009	Sheet 35 of 53

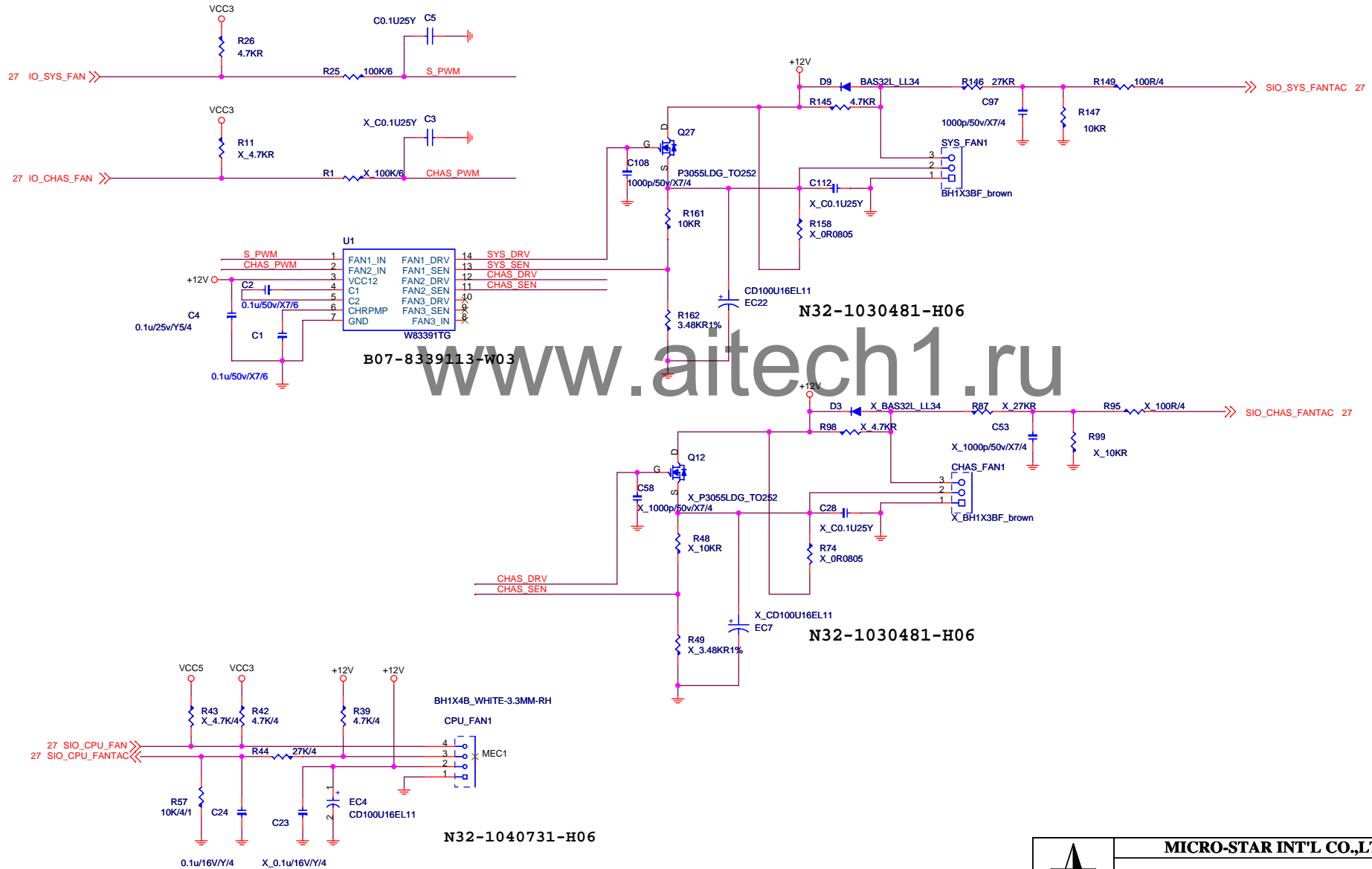
www.aitech1.ru



DVI level shifter

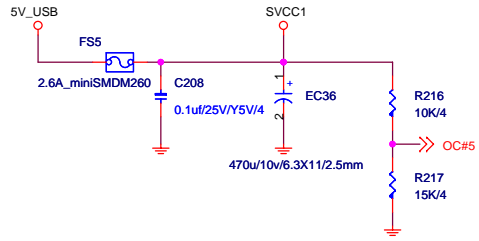


FAN-COUNTROL CIRCUIT

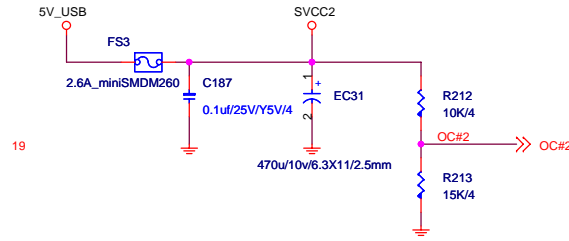


MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size	Document Description	Rev
Custom	FAN Control	10
Date: Tuesday, July 21, 2009		Sheet 38 of 53

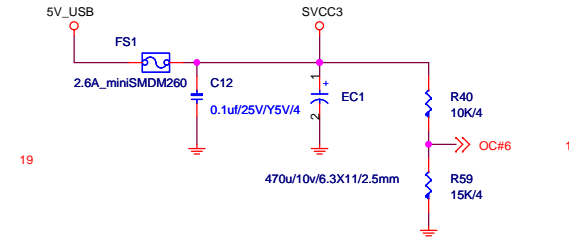
POWER CIRCUIT FOR USB PORT 10, 11



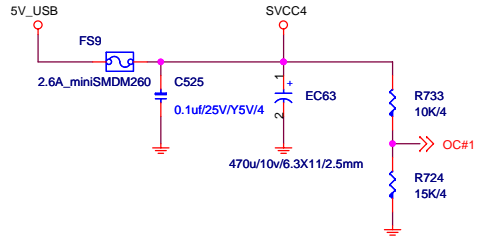
POWER CIRCUIT FOR USB PORT 4, 5



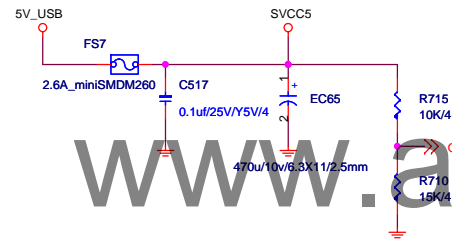
POWER CIRCUIT FOR USB PORT 12, 13



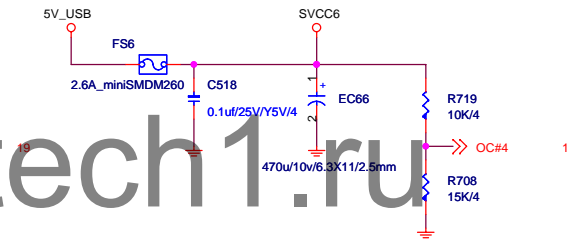
POWER CIRCUIT FOR USB PORT 2, 3



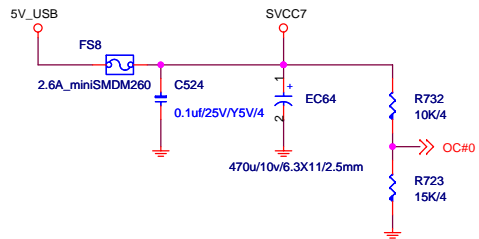
POWER CIRCUIT FOR USB PORT 6, 7



POWER CIRCUIT FOR USB PORT 8, 9



POWER CIRCUIT FOR USB PORT 0, 1



www.aitech1.ru



MICRO-STAR INT'L CO.,LTD

MS-7613

Size Custom	Document Description USB POWER	Rev 10
Date: Tuesday, July 21, 2009	Sheet 39 of 53	

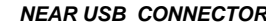
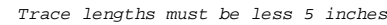
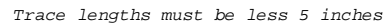
Trace lengths must be less 12 inches



Trace lengths must be less 12 inches



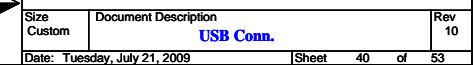
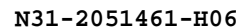
Trace lengths must be less 5 inches



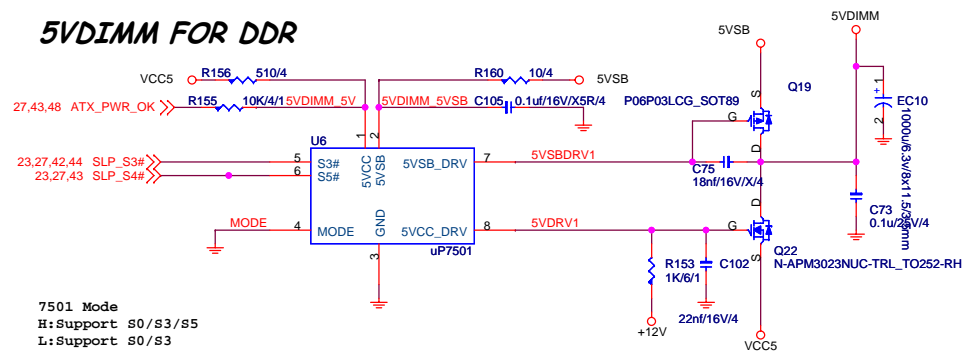
Trace lengths must be less 5 inches



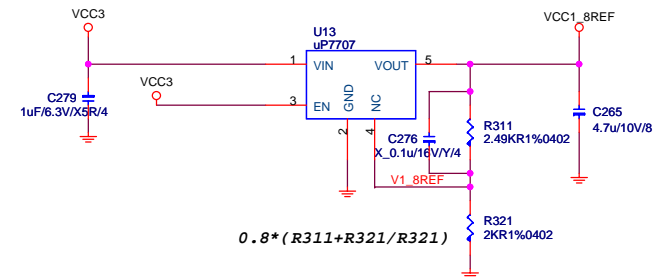
Trace lengths must be less 5 inches



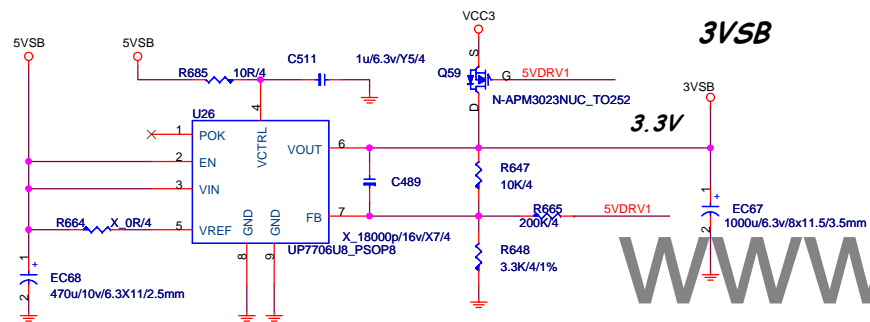
5VDIMM FOR DDR



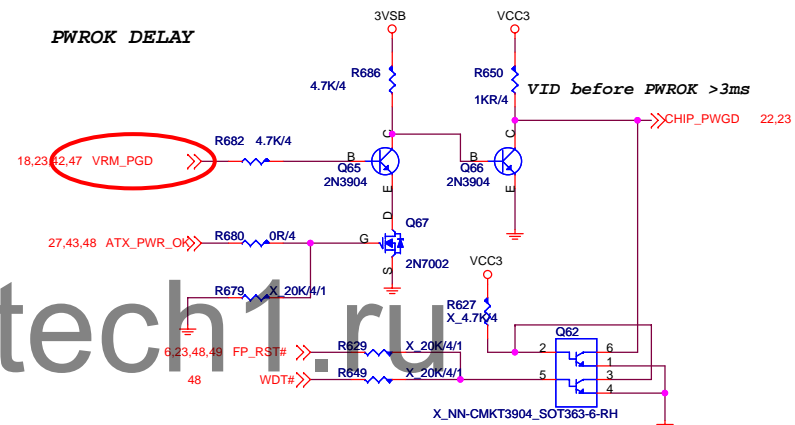
VCC1_8REF



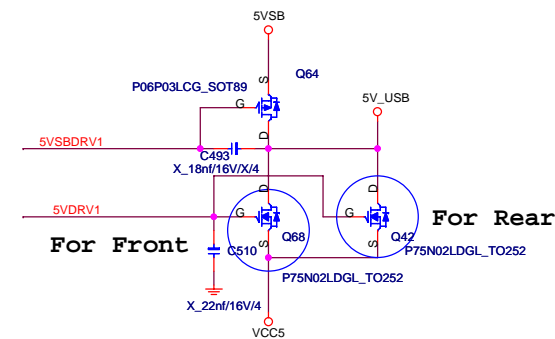
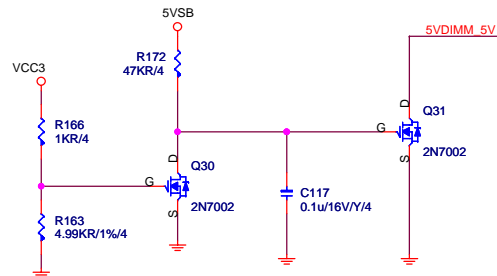
3VSB



PWROK DELAY



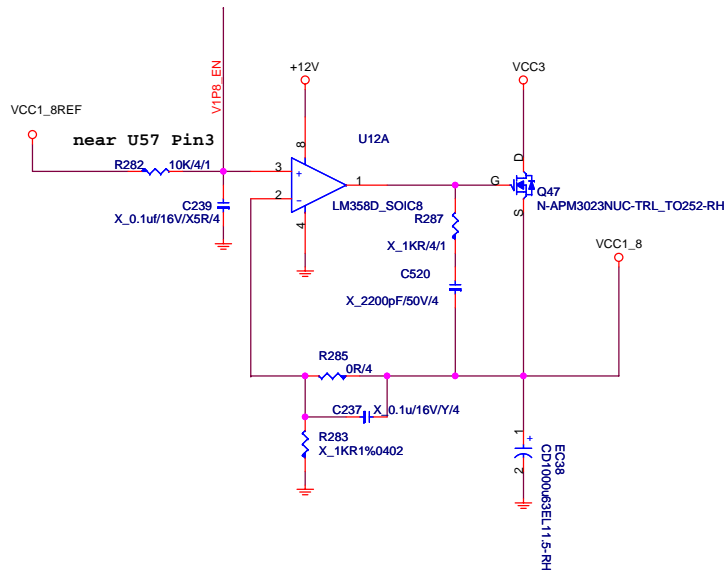
Update from SLP_S3# to VRM_PGD



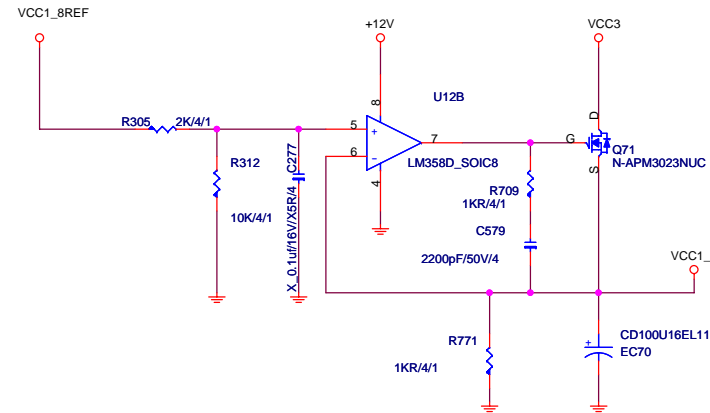
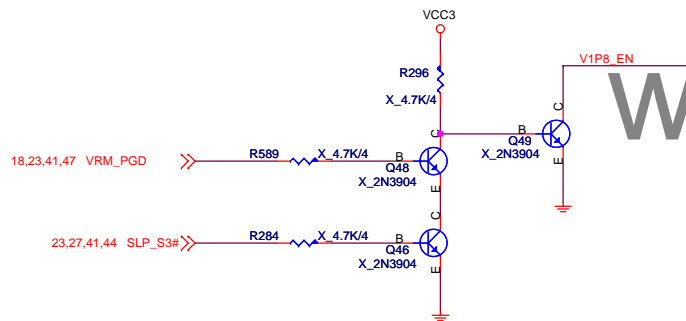
MICRO-STAR INT'L CO.,LTD

MS-7613

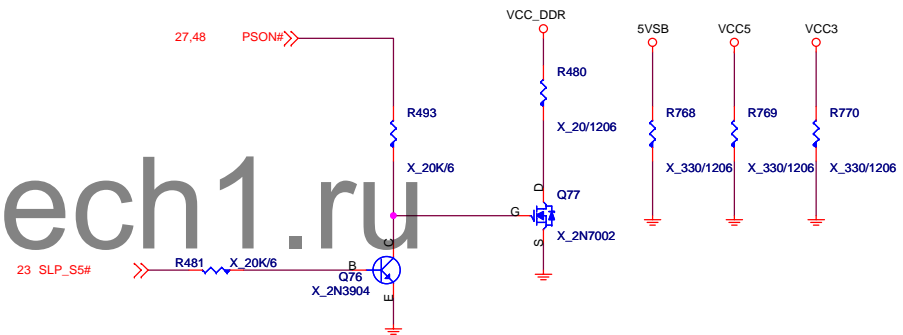
Size Custom	Document Description ACPI Controller 1	Rev 10
Date: Tuesday, July 21, 2009		Sheet 41 of 53



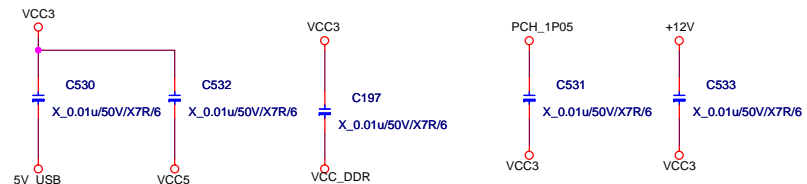
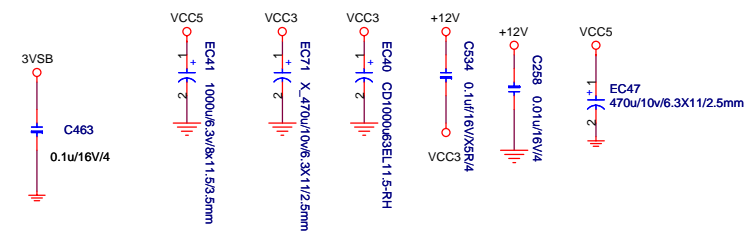
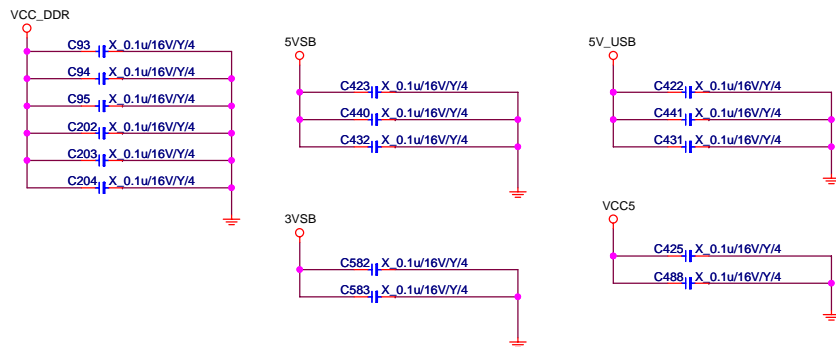
cpuvtt & pch vore wait 1.8v



Discharge Circuit



For EMI

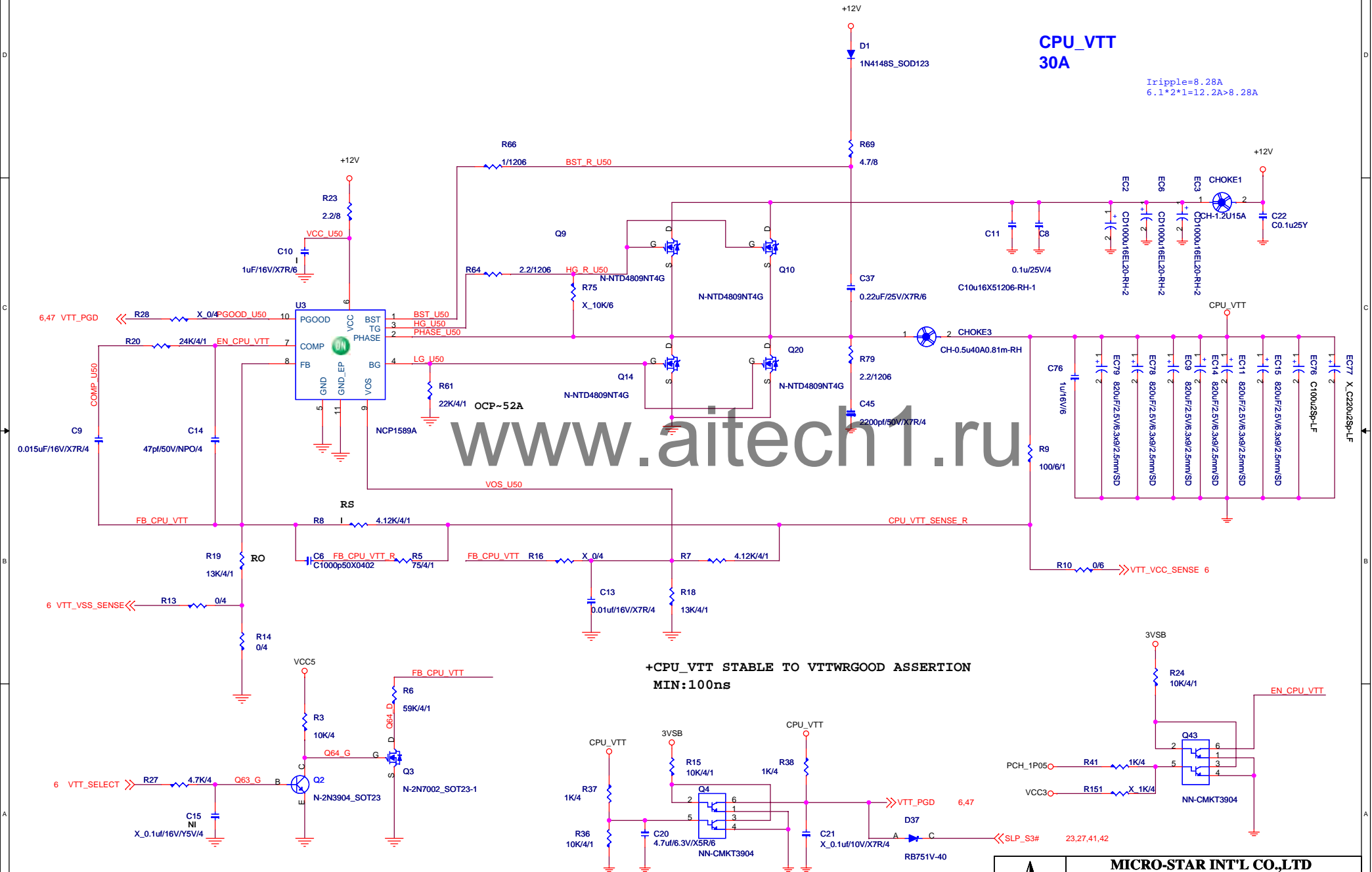


MICRO-STAR INT'L CO.,LTD

MS-7613

Size	Document Description	Rev
Custom	ACPI Controller 2	10
Date:	Tuesday, July 21, 2009	Sheet 42 of 53

VTTWRGD LEVEL SHIFT



CPU_VTT
30A

Iripple=8.28A
6.1*2*1=12.2A>8.28A

+CPU_VTT STABLE TO VTTWRGD ASSERTION
MIN:100ns



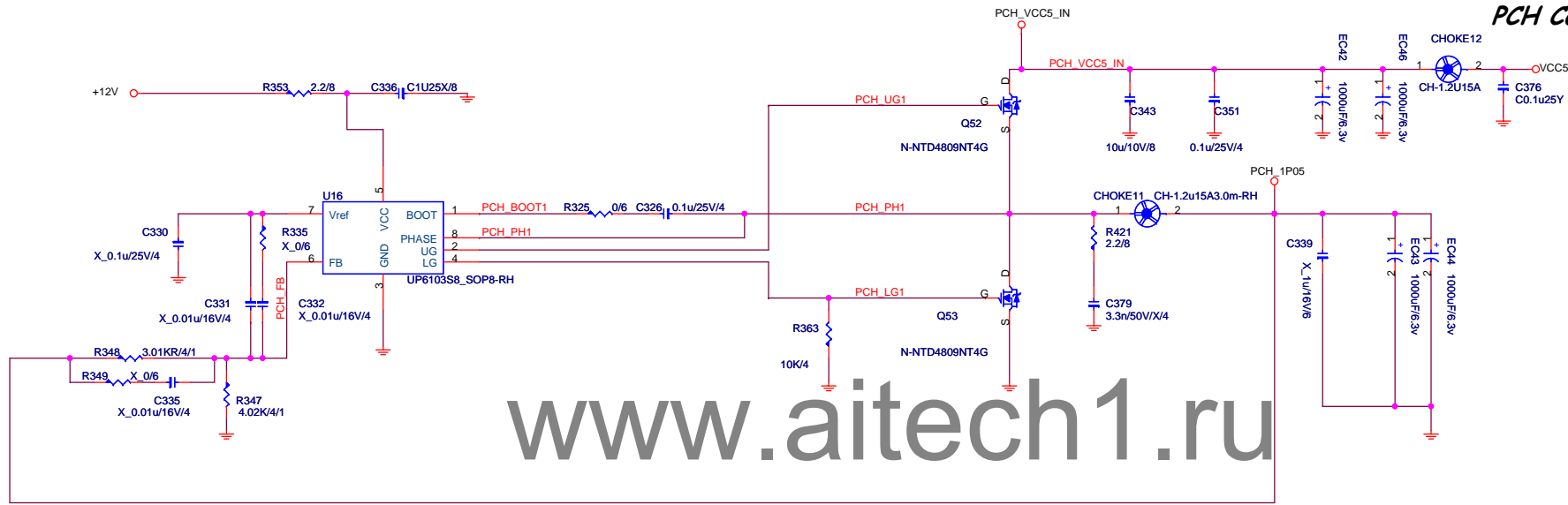
MICRO-STAR INT'L CO.,LTD

MS-7613

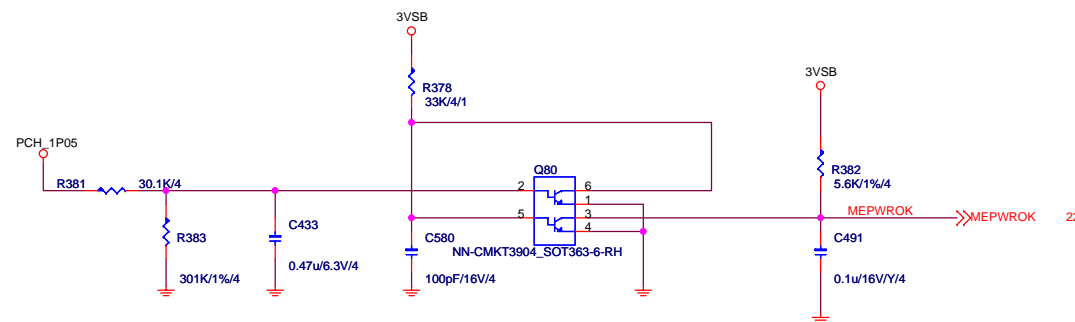
Size	Document Description	Rev
Custom	CPU_VTT - NCP1589A_1-Phase	10
Date: Tuesday, July 21, 2009	Sheet 44 of 53	

5.5A+2.5A(VCCME)=8A

PCH Core



www.aitech1.ru



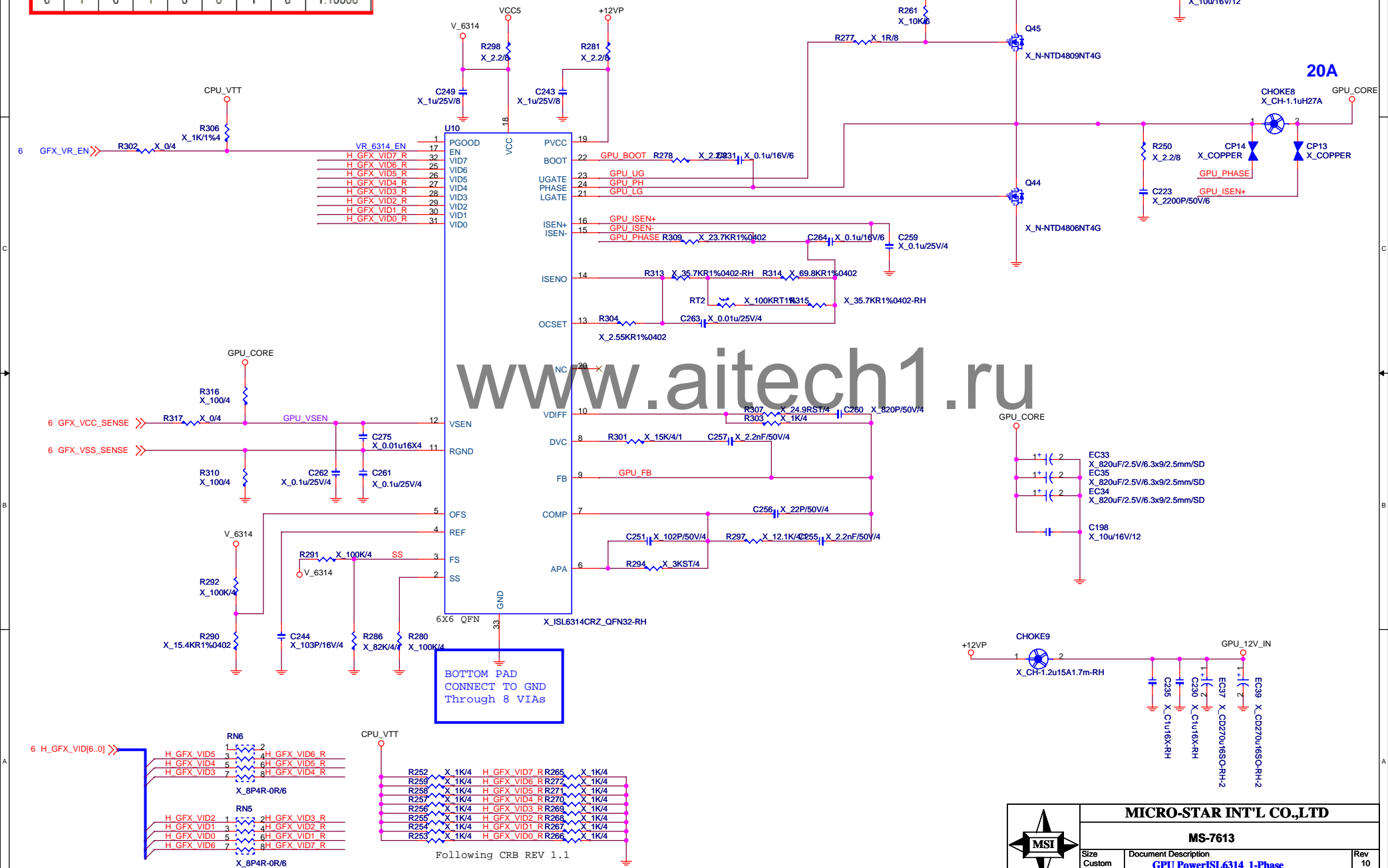
MICRO-STAR INT'L CO.,LTD

MS-7613

Size	Document Description	Rev
Custom	PCH POWER - UPI6103_1-Phase	10
Date: Tuesday, July 21, 2009	Sheet 45 of 53	

***GPU_CORE* 20A**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000

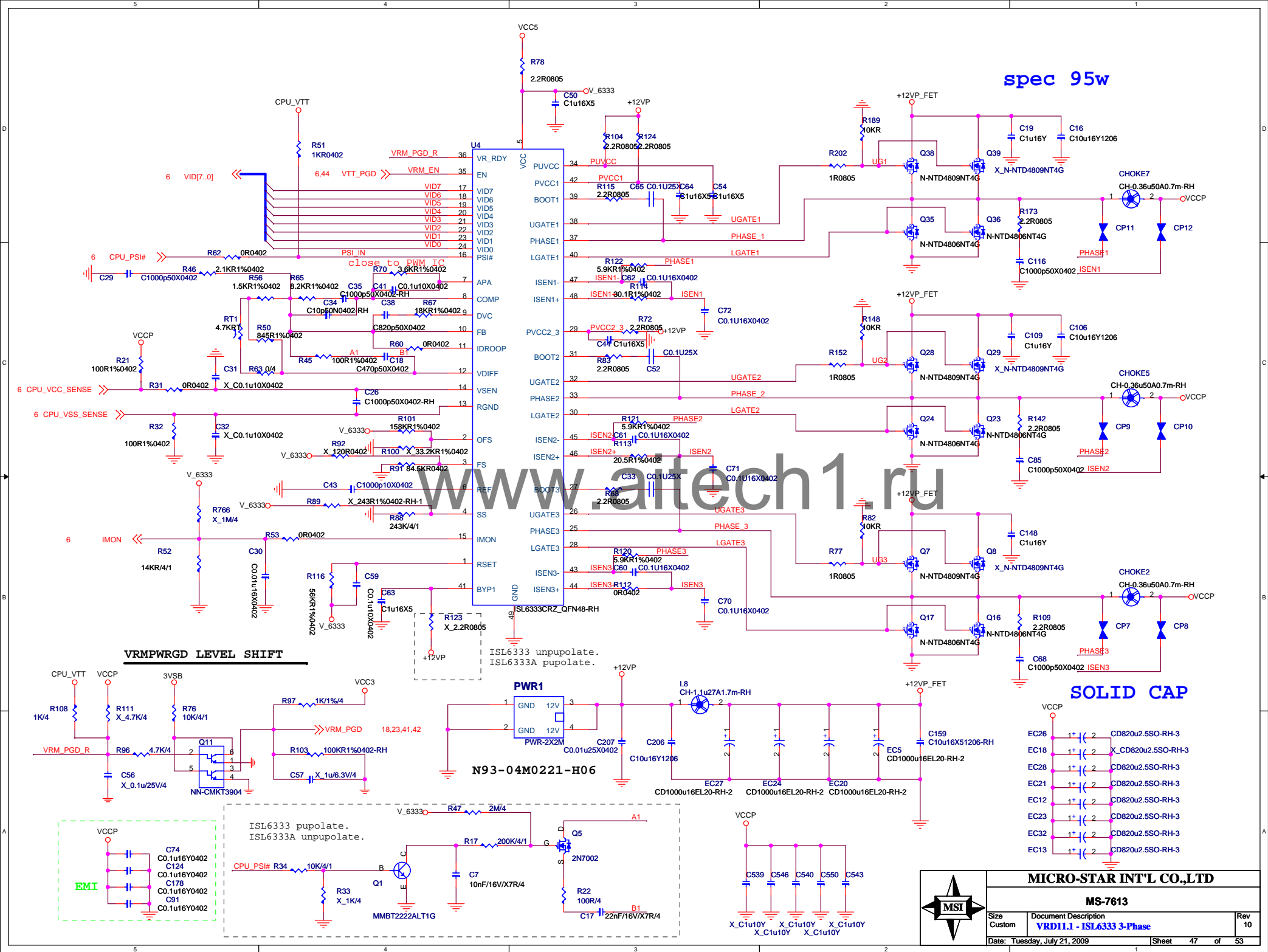


MICRO-STAR INT'L CO.,LTD

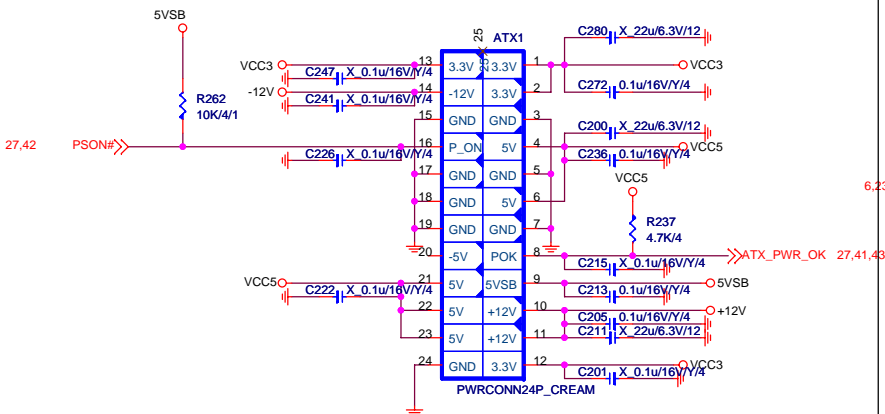
MS-7613

Size Custom	Document Description GPU PowerISL6314 1-Phase
----------------	---

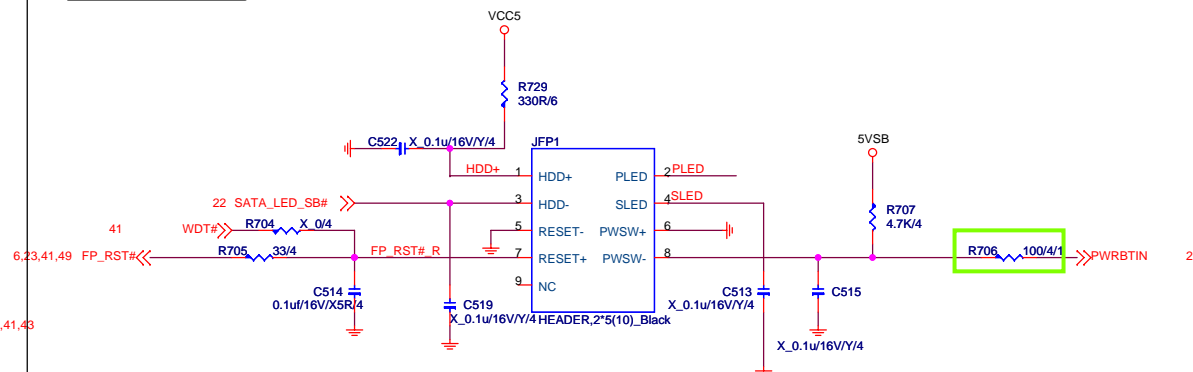
Rev	10
-----	----



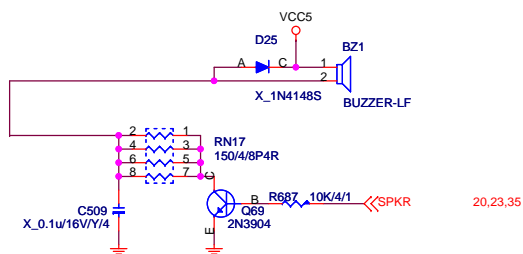
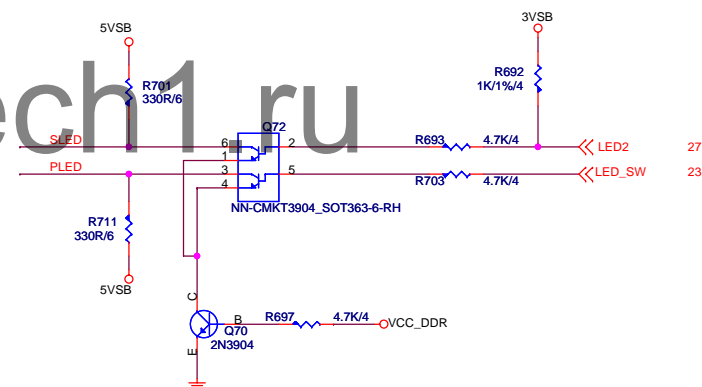
ATX POWER CONNECTOR



FRONT PANNEL



LED



	Single color LED		Dual color LED	
	LED2	LED_SW	LED2	LED_SW
S0	H	L	H	L
S1/S3	Blinking	L	L	H
S4/S5	L	L	L	L



MICRO-STAR INT'L CO.,LTD

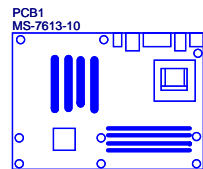
MS-7613

Size Custom Document Description ATX PWR-Connector/LED

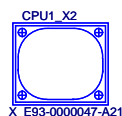
Rev 10

Date: Tuesday, July 21, 2009 Sheet 48 of 53

PCB



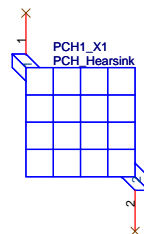
P30-0761310-G37



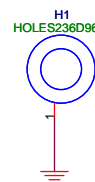
X_E93-0000047-A21



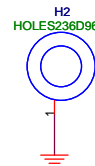
BAT-BCR2032P-RH



E31-0401634-K08

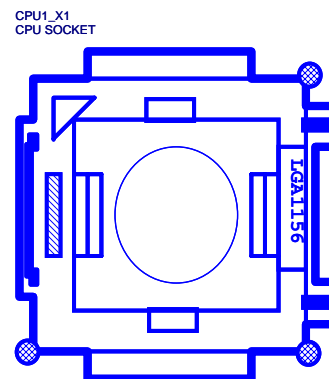


H1
HOLES236D96



H2
HOLES236D96

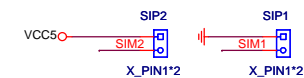
CPU SOCKET



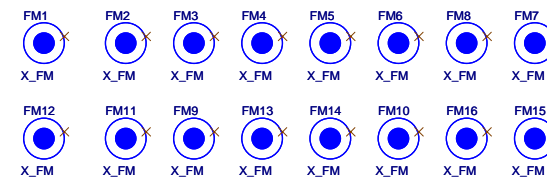
CPU1_X1
CPU SOCKET

E21-7557010-F02

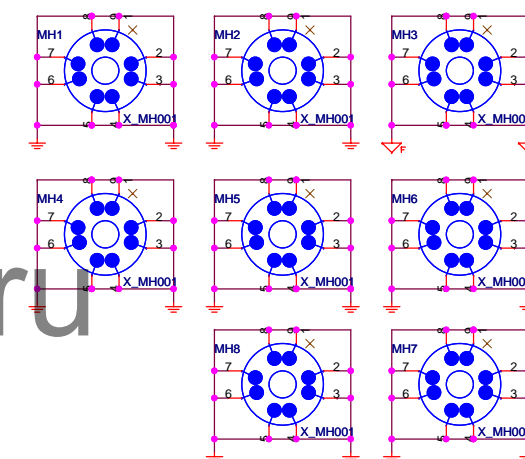
Simulation



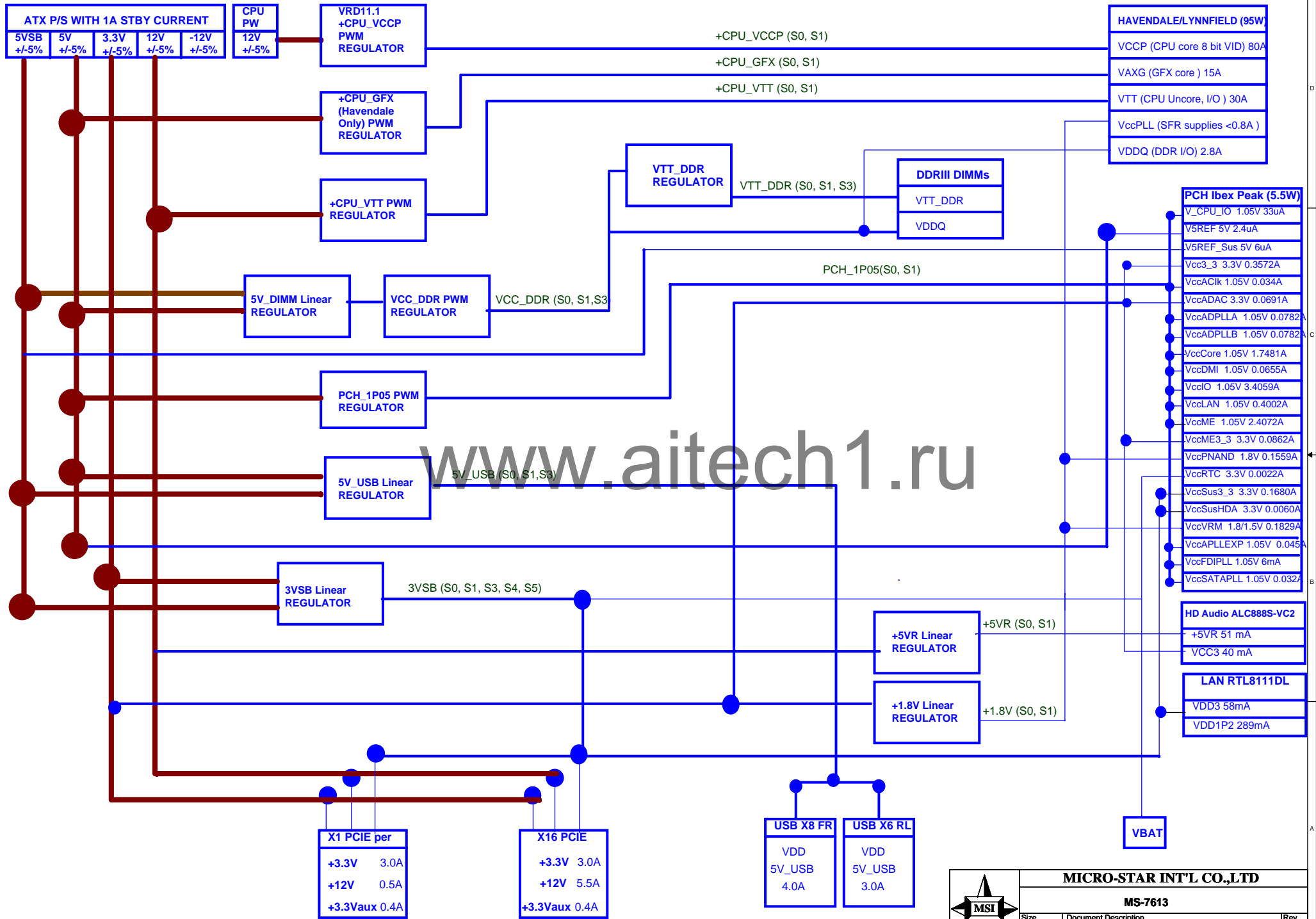
Optical Fiducial Marks-120



Mounting Holes



www.aitech1.ru



Version 0A:

2009/03/16
Page 23: Populate R668 by Intel suggestion.
Page 23: Populate 100k ohm in R668 by Intel suggestion.
Page 23: Unpopulate R214 by Intel suggestion.

Version 0B:

2009/03/17
Page 35: Add internal amplifier circuit by HP requestion.
Page 34: Remove internal line-in circuit by HP requestion.
Page 6: Add CPU POC circuit following Design guide..
Page 47: Change R123 to 2.2ohm/0805 reserve for ISL6333A.
Page 39: Change USB port 0, 1 OC from OC#5 to OC#0 following Design guide.
Page 36: Change R143 and R140 from 100 ohm to 0 ohm by Intel suggestion.
Page 23: Pull-up GPIO57 to 3VSB by Intel suggestion.
Page 23: Unpopulate R603 by Intel suggestion.
Page 23: Pull-up SML0CLK and SML0DATA to 3VSB by Intel recommend.
Page 23: Pull-up SMBCLK and SMBDATA to 3VSB by Intel recommend.
Page 23: Swap HAD_SYNC and HAD_RST to match ball name.
Page 23: Connect PCH_JTAGRST# to a test point by Intel recommend.
Page 49: Connect SATA4GP to Pin 34 of the JTAG connector by Intel recommend.
Page 49: Connect Pin 41 of the JTAG connector to a test point by Intel recommend.
Page 49: Connect VCC of the JTAG connector to 3VSB by Intel recommend.
Page 23: Connect GIOP26 to control audio de-pop circuit.
Page 23: Use GIOPI3 to switch audio Verb Table with internal amplifier or not.
Page 37: Reserve R512 for DVI level shifter eable control.
2009/03/19
Page 20: Change R539 and R546 from 39 ohm to 22 ohm by Intel recommend.
Page 27: Reserve R766 for RSMRST# timing control.
Page 23: Change GPIO45, GPIO46, GPIO47 pull-up well from VCC3 to 3VBS following schematic checklist.
Page 22: Connect SATA port4 to SATA5 connector by HP recommend.
Page 22: Connect SATA port2 to SATA3 connector by HP recommend.
Page 22: Use GPIO22, GPIO38, GPIO39, GPIO48 for MB_ID.
Page 32: Unpopulate C216 for EEPROM can not be programed issue.
2009/03/20
Page 42: Reserve discharge circuit.
Page 47: Connect IMON pin of VRD to ISENSE of CPU.
2009/03/23
Page 32: Unpopulate C209, C210, C214 to fix LAN LED wrong.
Page 42: Add R771 approve VCC1_5 whitout load.
2009/03/24
Page 22: Delete SATA5, SATA6 connector.
Page 22: Change SATA1 and SATA2 to right angle connector.
Page 15: Change C160 to 22uF/0805 and add a 22uF/0805 in C470.

2009/03/25
Page 23: Change R595 from 10k ohm to 1k ohm.
Page 23: Reserve R561 to pull-up FP_RST# to 3VSB.
Page 30: Add R813 and R814 to switch Mini-card support wake function or not.
Page 41: Change R650 from 4.7k ohm to 1k ohm for approving CHIP_PWGD signal level.
2009/03/26
Page 34: Move D24 to pin2 of U27.
Page 34: Change R681 from 309 ohm to 324 ohm.
Page 34: Connect D32 to 3VSB.
Page 30: Add Wireless LED (JWLED) by HP requirement.

2009/03/27

Power solution:
Page 47: Change R50 from 681 ohm to 931 ohm.
Page 47: Change R56 from 1.24k ohm to 1.33k ohm.
Page 47: Change R101 from 162k ohm to 255k ohm.
Page 47: Change C34 from 33 pF to 10 pF.
Page 47: Change C35 from 470 pF to 1000 pF.
Page 47: Change R65 from 16.5k ohm to 21k ohm.
Page 47: Change R70 from 5.1k ohm to 3k ohm.
Page 12: Populate C96 and C98.
Page 47: Populate 4700pF cap in C29 and 2.49k ohm resistor in R46.
Page 47: Change R52 from 13.3k ohm to 14.3k ohm.
Page 47: Change CHOK2, CHOK5 and CHOK from 0.5uH to 0.36uH
Page 47: Populate EC32.
Page 47: Change R120, 121 and R122 from 6.19k ohm to 5.11k ohm.
Page 44: Change C6 from 0.015uF to 4700pF.
Page 44: Change R8 from 4.32k ohm to 4.12k ohm.
Page 44: Populate 820uF cap in EC78.
Page 44: Change EC76 from 100uF to 220uF and non-stuff EC77.
Page 44: Add a 820uF cap in EC79.

2009/03/30

Page 23: Change R642 from 4.75k ohm to 1.1k ohm.
and R641 from 12.1k ohm to 3k ohm following Intel MOW WW13 2009.
Page 27: Change R571 from 5.6k ohm to 5.9k ohm to meet RSMRST# falling spec.
and unpopulate C456 to meet RSMRST# falling spec.


2009/03/31

Page 20: Reserve C471, C479 and C483 for EMI.
2009/04/02
Page 26: Un-stuff R431 and R400.
Stuff R423, R401, R367, R475, R374 and R450 for using external LC filter.
Page 38: Connect Pin 1 of U1 to fix system fan always full on.
Page 48:Use GPIO31 to control power LED for LED turn red then green with dual color LED.

2009/04/06

Page 33: Reserve C485 for AZ_SDOUT.
2009/04/07
Page 34: Reserve Q78, Q79, R773, C475, R702, R773 for power saving in S5.
Page 43: Change R200 from 1.3k ohm to 1.33k ohm for DDR power quality.
Page 27: Add D36 and connect to ATX_PWR_OK for AC power lost last state function adnormal.
2009/04/09

Page 18: Change Clock gen from realtek RTM875N-606 to realtek RTM885N-932.
Page 44: Add D37 to fix CPU_VTT leakage in S3 state.



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size Custom	Document Description History	Rev 10
Date: Tuesday, July 21, 2009		Sheet 52 of 53

Version 0C:

2009/04/21

Page 23: Reserve C365 to fix sometime the system auto wake when insert PCIE device.

Page 27: Connect KBRST# and A20GATE of IO to PCH KBRST# and A20GATE.

Page 23: Use GPIO44 to control onboard LAN power.

2009/04/27

Page 28: Add C412 for PCIE slot power.

Page 34: Reserve C419 for audio power.

2009/05/06

Page 40: Leave pin10 of JUSB1 and JUSB2 NC for some card reader work abnormal.

Page 41: Change EC67 to 1000uF for 3VSB power quality.

Page 37: Swap DVI_TXD2+ and DVI_TXD2-.

2009/05/07

Power Solution:

Page 12: Unpopulate C146, C139, C181

Page 12: Unpopulate C142, C155, C168, C171, C179, C176, C167, C145

Page 44: Change EC76 from 220uF to 100uF.

Page 44: Change C6 from 4700pF to 1000pF.

Page 47: Change R101 from 255k ohm to 158k ohm.

Page 47: Change C18 from 680 pF to 470pF.

Page 47: Change R70 from 3k ohm to 2.74k ohm.

Page 47: Change R120, R121 and R122 from 5.1k ohm to 5.9k ohm.

Page 47: Change C29 from 4700 pF to 1000pF.

Page 47: Change R46 from 2.49k ohm to 2.1k ohm.

Page 47: Change R45 from 750 ohm to 100 ohm.

Page 47: Change R65 from 2.1k ohm to 8.2k ohm.

Page 47: Change C35 from 1000 pF to 3300pF.

Page 47: Change R52 from 14.3k ohm to 14k ohm.

Page 47: Change R56 from 1.33k ohm to 1.4k ohm.

Page 46: Change R290 from 9.1k ohm to 15.4k ohm.

Page 46: Change R309 from 19.6k ohm to 23.7k ohm.

Page 46: Change R286 from 100k ohm to 82k ohm.

2009/05/11

Page 18: Change clock gen from RTM885N-932 to Silego SLG8SP585

Page 27: Change R571 from 5.9K ohm to 5.6K ohm for meet RSMRST# falling time.

Page 12: Populate 0 ohm in C186 following WW16 MoW

(Discrete graphic only support, VAXG tie to GND)

Page 11: Populate R293, R299 following WW18 MoW

Page 30: Connect LED_WLED to pin4 of JWLED for meet LED cable define.

Page 22: Change SATA1 and SATA2 connector type to DIP.

2009/05/18

Page 23: Change C495 and C500 from 10pF to 18pF.

Page 13, 15: Change C137 and C161 from 0.1uF to 2.2uF to improve Vref_CA power.

Page 30: Reserve R780 for mini card.

Page 30: Connect R813 to 3VSB_SLOT.

Page 21: Add R375 and R376 for support two TL-399.

2009/05/26

Page 23: Populate R619 to fix TV tuner card can't be detected when system restart.

2009/06/16

Power Solution:

Page 46: Un-stuff R33.

Page 46: Change R50 from 931 ohm to 845 ohm.

Page 46: Change R56 from 1.4K ohm to 1.5K ohm.

Page 46: Change R70 from 2.74K ohm to 3.6K ohm.

Page 46: Change C35 from 3300 pF to 1000 pF.

Page 46: Stuff 1000 pF in C26.

Page 44: Change R6 from 69.8K ohm to 59K ohm.

2009/06/22

Page 24: Un-stuff C560

Page 24: Change C557 to 0 ohm.

2009/06/25

Page 39: Change R216,R212,R40,R733,R715,R719,R732 from 220 ohm to 10K ohm.

Page 39: Change R217,R213,R59,R723,R710,R708,R723 from 330 ohm to 15K ohm.

Version 0D:

2009/06/22

Page 45: Add MEPWRGD circuit.

2009/06/25

Page 23: Add RECOVERY header.

2009/06/26

Page 37: Reserve C581 for EMI.

2009/06/30

Page 20: Reserve R393 and R395.

2009/07/02

Page 42: Reserver C582 and C583 for EMI.

Page 49: Reserve R545,R782,R783 and R784.

2009/07/09

Page 49: Un-stuff R579,R558,R543,R584,R568,R534.

2009/07/14

Power Solution:


Page 44: Un-stuff R16.

Page 44: Stuff 4.12k ohm in R7.

Page 44: Stuff 13k ohm in R18.

Page 44: Stuff 0.01uF in C13.

www.aitech1.ru



MICRO-STAR INT'L CO.,LTD		
MS-7613		
Size Custom	Document Description History	Rev 10
Date: Tuesday, July 21, 2009		Sheet 53 of 53